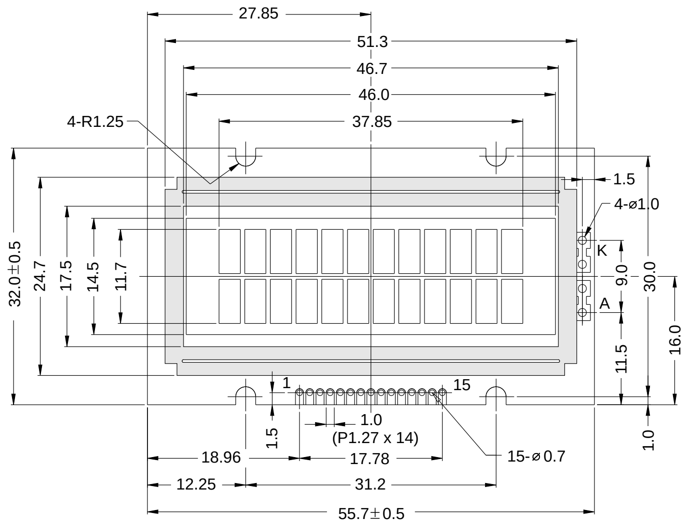
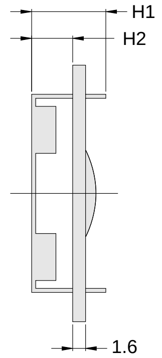
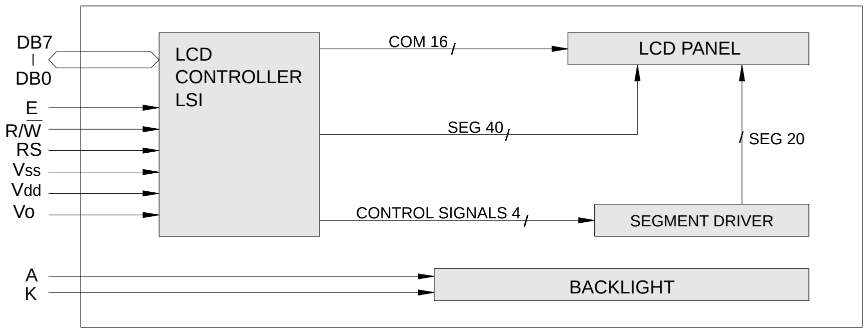
PC 1202-A

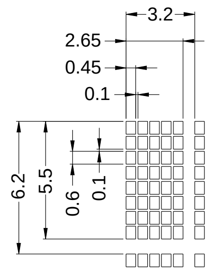


OUTLINE DIMENSION & BLOCK DIAGRAM









The tolerance unless classified ±0.3mm

MECHANICAL SPECIFICATION			
Overall Size	55.7 x 32.0	Module	H2 / H1
View Area	46.7 x 17.5	W /O B/L	5.1 / 9.2
Dot Size	0.45 x 0.60	EL B/L	5.1 / 9.2
Dot Pitch	0.55 x 0.70	LED B/L	8.7 / 12.8

PIN ASSIGNMENT

Pin no.	Symbol	Function
1	Vss/K	Power supply(GND) / LED B/L(–)
2	Vdd	Power supply(+)
3	Vo	Contrast Adjust
4	RS	Register select signal
5	R/$\overline{W}$	Data read / write
6	E	Enable signal
7	DB0	Data bus line
8	DB1	Data bus line
9	DB2	Data bus line
10	DB3	Data bus line
11	DB4	Data bus line
12	DB5	Data bus line
13	DB6	Data bus line
14	DB7	Data bus line
15	A	Power supply for LED B/L (+)

ABSOLUTE MAXIMUM RATING

Item	Symbol	Condition	Min.	Max.	Units
Supply for logic voltage	Vdd-Vss	25°C	-0.3	7	V
LCD driving supply voltage	Vdd-Vee	25°C	-0.3	13	V
Input voltage	Vin	25°C	-0.3	Vdd+0.3	V

ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min.		Typical		Max.		Units
Power supply voltage	Vdd-Vs	25°C	2.7		–		5.5		V
LCD operation voltage	Vop	Top	N	W	N	W	N	W	V
		-20°C	–	7.1	–	7.5	–	7.9	V
		0°C	4.5	–	4.6	–	5.1	–	V
		25°C	4.1	6.1	4.4	6.4	4.7	6.7	V
		50°C	3.8	–	4.1	–	4.4	–	V
		70°C	–	5.7	–	6	–	6.3	V
LCM current consumption (No B/L)	Idd	Vdd=5V	–		1.5		2.5		mA
Backlight current consumption	LED/edge	VB/L=4.2V	–		40		–		mA
	LED/array	VB/L=4.2V	–		80		–		mA

REMARK

LCD option: STN, TN, FSTN

Backlight Option: LED Backlight feature, other Specs not available on catalog is under request.

● CODING SYSTEM FOR LCD MODULE

P	C	1 6	0 2	*	*	*	-	*	*	-	*	-	*
1	2	3	4	5	6	7		8	9		10		11

NO	Code value	Description	Type
1	P	Powertip products	Brand
2	C	Character	Module type
	G	Graphic	
	S	Engineer sample	
	T	Total solution	
3	08.16.20.24 ···	Characters per line (for character modules)	Characters per line or row dots
	120.122.128 ···	Row dots (for graphic modules)	
4	01.02.03.04 ···	Lines (for character modules)	Lines or column dots
	32.64.128 ···	Column dots (for graphic modules)	
5	A	Without backlight	Backlight mode (Type + Color)
	B	EL backlight, Blue-green	
	D	EL backlight, Yellow-green	
	E	EL backlight, White	
	F	CCFL backlight, White	
	L	LED backlight, Yellow-green	
	M	LED backlight, Amber	
	N	LED backlight, Red	
	O	LED backlight, Orange	
	P	LED backlight, Pure-green	
	S	LED backlight, Green	
	U	LED backlight, Blue	
	W	LED backlight, White	
6	R	Standard (through hole, cable, connector and etc.)	Connecting type
	Y	Straight pin-header	
	Z	Right angle pin-header	
7	None (*1)	TN positive, Gray	LCD mode (Type + Color)
	N	TN negative, Blue	
	S	STN positive, Gray	

7	U	STN positive, Yellow-green	LCD mode (Type+Color)
	M	STN negative, Blue	
	F	FSTN positive, White	
	T	FSTN negative, Black	
8	0~Z	Series number	Model name
9	00~ZZ	IC manufacturer / character pattern /total solution series number	* 2
	NN	Without controller	
10	A	Reflective /Normal temp. /6:00 direction	Polarizer type/ LCD Temperature range/ Viewing direction
	D	Reflective /Normal temp. /12:00 direction	
	G	Reflective /Extended temp. /6:00 direction	
	J	Reflective /Extended temp. /12:00 direction	
	B	Transflective /Noraml temp. /6:00 direction	
	E	Transflective /Noraml temp. /12:00 direction	
	H	Transflective /Extended temp. /6:00 direction	
	K	Transflective /Extended temp. /12:00 direction	
	C	Transmissive /Normal temp. /6:00 direction	
	F	Transmissive /Normal temp. /12:00 direction	
	I	Transmissive /Extended temp. /6:00 direction	
	L	Transmissive /Extended temp. /12:00 direction	
11	No code value	Standard product	Version
	01~ZZ	Special code	

(*1) Without code value

(*2)

Character Pattern	Character							Graphic	
English / Japanese	EA	HO/HA/HC	SO	NO	WA	AO	JA	YA	E4
English / Europe	EB	H2/HB/HC/HU	S5/S6	N5/N6/NI	WB/W5		JB	TA	
English / France	EC		S3	N3					
English / Russia	EH		SH	NH					
English / Chinese		HH							
English / Hebrew			S4/S8	N4/N8					

Note:

A: APANPEC LSI
M: MOTOROLA LSI
R: SHARP LSI
W: SITRONIX LSI
E: ESPON LSI
N: NOVATECH LSI
S: SUMSUNG LSI
Y : SANYO LSI
H: HITACHI LSI
O: OKI LSI
T: TOSHIBA LSI
J : JRC LSI
P: PHILIPS LSI
U: UMC GROUP LSI

(*3) Check with our sales for available combinations.

POWERTIP

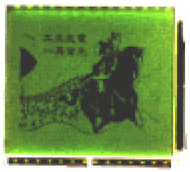
● CODING SYSTEM FOR OTHER PRODUCTS

P D - ＊ ＊ ＊ ＊ ＊ ＊

1 2

NO	CODE VALUE	DESCRIPTION	TYPE
1	PD	Powertip design product	Products
2	IN05300,IN05500...	Product characteristic	Types

NOTE:The code value and length of product characteristic are unlimited



Technical

POWERTIP TECHNOLOGY, INC.
DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Typtical / Electrical Characteristics of LCD Modules

- Optical Characteristics Of LCD Modules
- Electrical Characteristics Of LCD Modules

Optical Characteristics Of LCD Modules

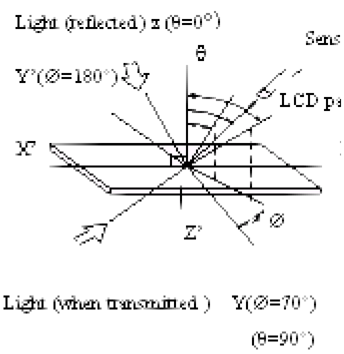
STN Type, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Note
Viewing angle	θ2-θ1	C≥2.0,∅=0°C	60°	-	-	Note 1,2
Contrast Ratio	C	θ=5°, ∅=0°	-	5	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-	150ms	250ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	200ms	300ms	Note 4

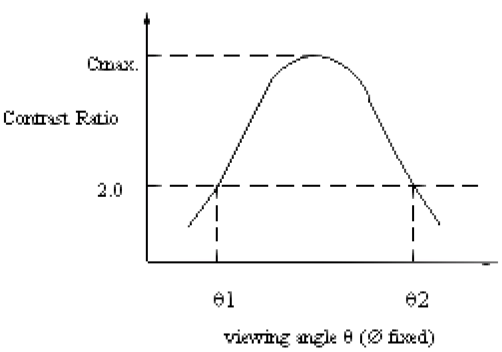
TN Type, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Note
Viewing angle	θ2-θ1	C≥2.0,∅=0°C		40°	-	Note 1,2
Contrast Ratio	C	θ=25°, ∅=0°	-	5	-	Note 3
Response time(rise)	ton	θ=25°, ∅=0°	-	80ms	120ms	Note 4
Response time(fall)	toff	θ=25°, ∅=0°	-	60ms	90ms	Note 4

Note 1: Definition of angles θ an

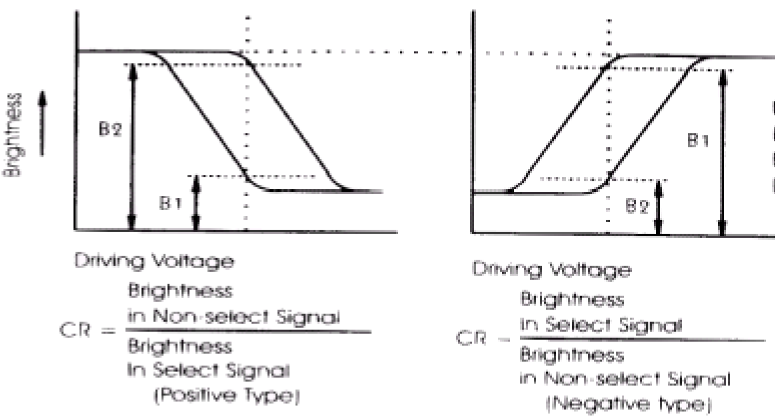


Note 2: Definition of viewing angles θ1 and θ2

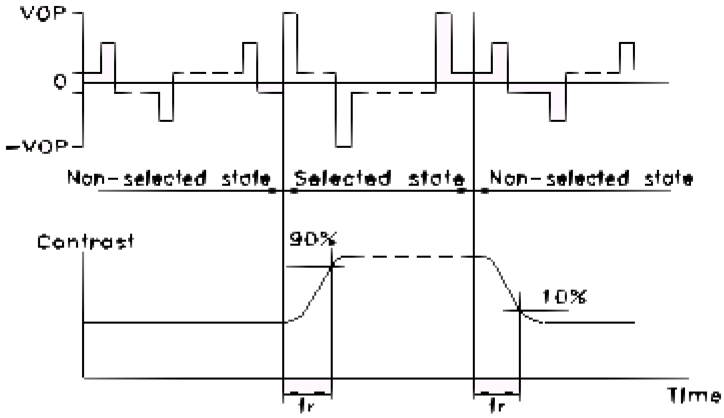


Remark: Optimum viewing angle with the naked eye and viewing angle θ at Cmax

Note 3: Definition of contrast Ratio



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm²

Vopr : Operating voltage fFRM : Frame frequency

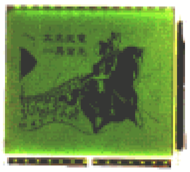
ton : Response time (rise) toff : Response time (fall

Electrical Characteristics Of LCD Modules

Character Type: V_{DD}=+5V±10%,V_{SS}=0V,T_A=25°C

Item	Symbol	Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Logic Supply voltage	V_{DD}	-	4.5	5	5.5	V
"H" input voltage	V_{IH}	-	2.2	-	V_{DD}	V
"L" input voltage	V_{IL}	-	0	-	0.6	V
"H" output voltage	V_{OH}	-	V_{DD}-0.3	-	-	V
"L" output voltage	V_{OL}	-	-	-	0.4	V
Supply current	I_{OP}	V_{DD}=5V	-	0.4	-	mA
LCD driving voltage	V_{LCD}	V_{DD}-V_O	3.0	8.1	11.0	V

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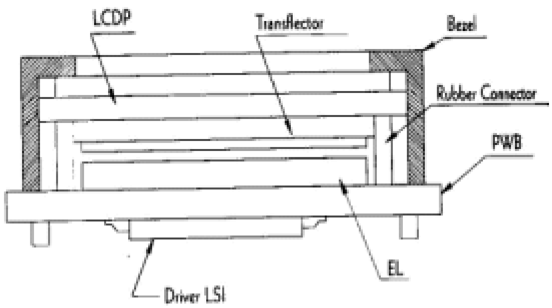
Backlight options for LCD modules

- EL Backlight
- CCFL Backlight
- LED Backlight

EL Backlight Precautions For Handling LCD Modules

Flat surface light source offers simple and even illumination over large area.

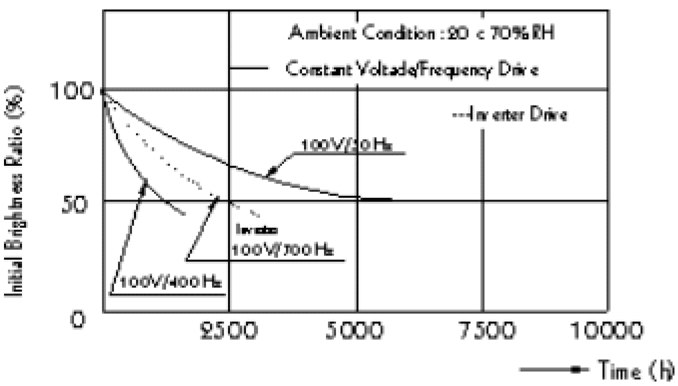
- Max.1.3mm thickness (Max. 1.5mm for lead portion)
- Wide driving condition, 60-1,000Hz at 150V AC Max. With inverter, step-up voltage from 1.5V battery is available.
- Emitted colors are blue-green, yellow-green and white.
- Operating characteristics of PC2002-A SERIES is 110V, 400Hz, 8mA, (Ta=20°C, 60% RHæ)
- Temperature Range:
  - Operating 0°C~ +50°C
  - Storage -20°C~ +60°C



Inverter for EL Backlight Drive:

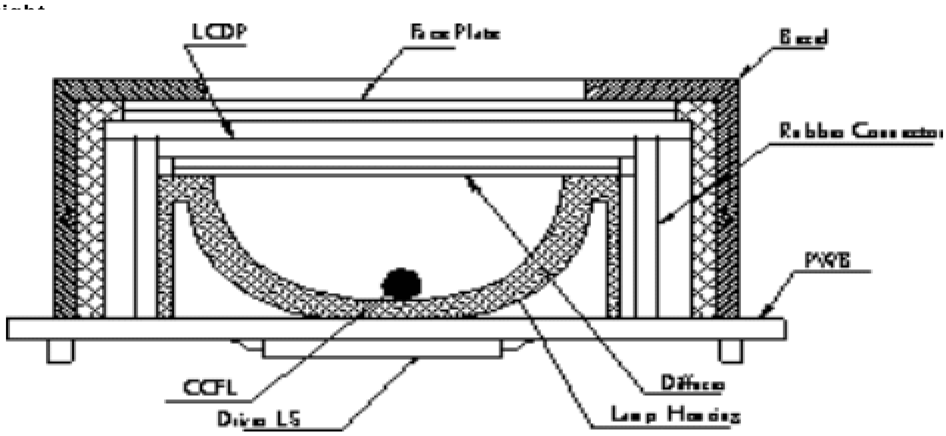
- Requires an inverter to operate the EL panel with a battery or DC power supply.
- Low inverter loss and high light efficiency since it is designed for EL backlight.
- Constant power consumption during operation, given temperature change for extended hours. This is characterized by the constant supply current, which minimizes the brightness change of the EL panel.

Life Characteristics:



CCFL Backlight(Cold Cathode Fluorescent Lamp)

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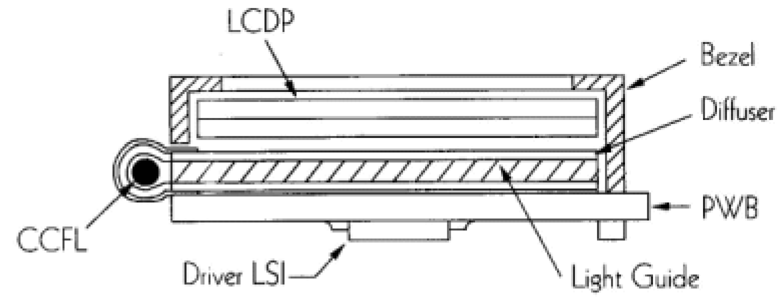
- High Brightness
- Long life time.
- Low Power consumption
- White color emitted

Direct Illumination

- Suitable for multi-color and / or dot matrix LCDP.

Edge Illuminatio

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  light source over a large area.



Precaution

- Inverter for CCFL use output high pressure AC current. Therefore, please pay attention when you handleinverter and power supply cable of LCD backlight.

LED Backlight

Long life, low power consumption and requires a simple power supply. Available colors are red, green and orange, available in array type illumination or edge illumination.

Features:

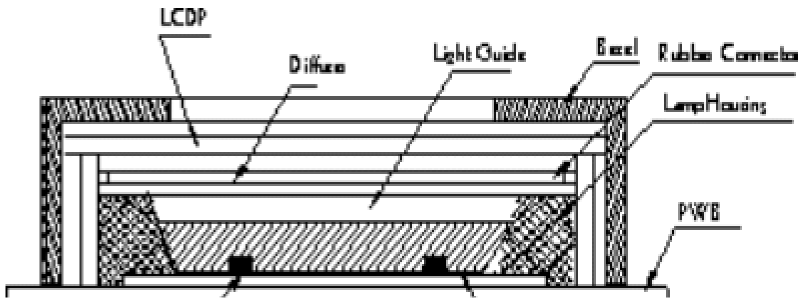
- Low driving voltage (DC) and does not require an inverter.
- Long life of 100,000 hours (average)
- No noise occurrence.

Various colors available in red, green and orange etc. (multi-color by alternative switch is also available)

- Operating characteristics of PC2002-A series is 4.2V, 210mA, 250cd/m

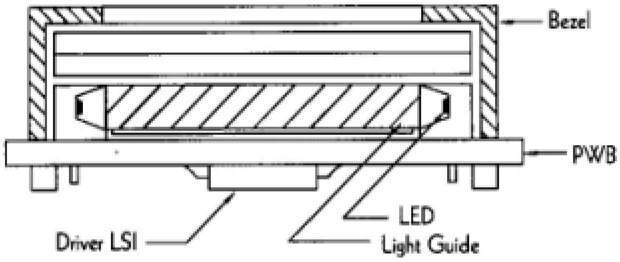
Array Illumina

-

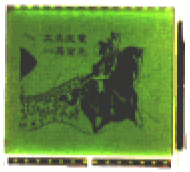


Edge Illumination

- Combination LED with a light guide offers a thin structure type of illumination.



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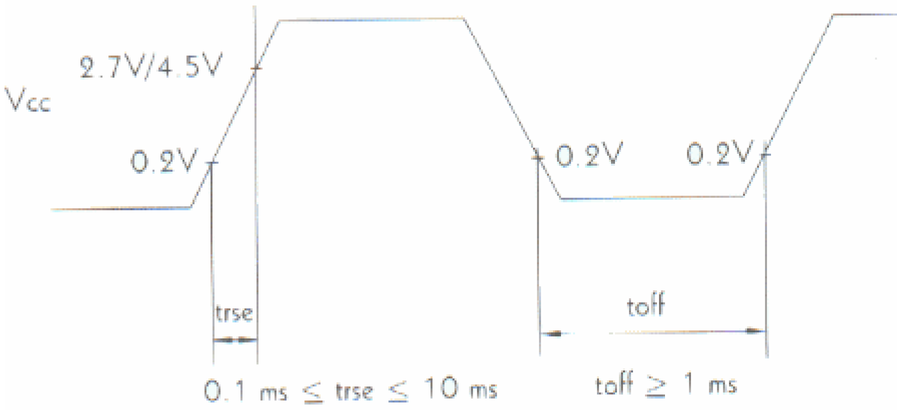


Technical

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Power Supply Reset

The internal reset circuit will be operating properly when the following power supply conditions are satisfied. If it is not operating properly, please perform the initial setting along with the instruction.



Item	Symbol	Measuring Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Power Supply RISE Time	trse	-----	0.1	-----	10	mS
Power Supply OFF Time	toff	-----	1	-----	-----	mS

Reset function

Initialization made by internal reset circuit

- The HD44780 automatically initializes (resets) when power is supplied (builtin internal reset circuit).
- The following instructions are executed during initialization.
  - The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10ms after Vdd reaches 4.5V.
    1. Display clear
    2. Function set
  - DL=1:8 bit long interface data
  - DL=0:4 bit F=0:5 * 7 dots character font
  - N=1:2 lines
  - N=0:1 line
    3. Display ON/OFF control
  - D=0:Display OFF C=0:Cursor OFF
  - B=0:Blink OFF
    4. Entry mode set
  - 1/D= 1:+1(increment) S=0:No shift

Note: When the power supply conditions, using internal reset circuit is not satisfied, the internal reset circuit will not function properly and initialization will not be performed.Please initialize using the MPU along with the instruction set.

Initialization along with instruction

If power supply conditions are not satisfied, for the proper operation of the internal reset circuit, it is necessary to initialize using the instructions.

Please use the following procedures.

Power ON — When interface is 8-bit long.

Wait more than 15ms after Vcc rise to 4.5V

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before the instruction
Function set (interface is 8 bits long)

Wait more than 4.1ms

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF Cannot be checked before the instruction
Function set (interface is 8 bits long)

Wait more than 100μs

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before the instruction
Function set (interface is 8 bits long)

BF cannot be checked before the following instructions. When BF is not checked. The waiting time between instructions is longer than the execution instruction time

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	N	F	*	*	Function Set(interface is 8 bit long. Specify the number of display lines and character font) The number of display line and character will be changed afterward.
0	0	0	0	0	0	1	0	0	0	Display OFF
0	0	0	0	0	0	0	0	0	1	Display ON
0	0	0	0	0	0	0	1	1/D	S	Entry Mode Set

Initialization ends.

Power ON — When interface is 4-bit long.

Wait more than 15ms after Vcc rise to 4.5V

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

BF cannot be checked before the instruction
Function set (interface is 4 bits long)

Wait more than 4.1ms

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

BF Cannot be checked before the instruction
Function set (interface is 4 bits long)

Wait more than 100μs.

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

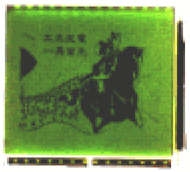
BF cannot be checked before the instruction
Function set (interface is 4 bits long)

BF cannot be checked before the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time.

RS	R/W	DB7	DB6	DB5	DB4	
0	0	0	0	1	1	Function Set(interface is 4 bits long. Specify the number of display lines and character font). The number of display lines and character will be changed afterward.
0	0	0	0	1	0	
0	0	N	F	*	*	
0	0	0	0	1	1	
0	0	1	0	0	0	Display OFF
0	0	0	0	1	1	
0	0	0	0	0	1	Display ON
0	0	0	0	1	1	
0	0	C	1	1/D	S	Entry Mode Set

Initialization ends.

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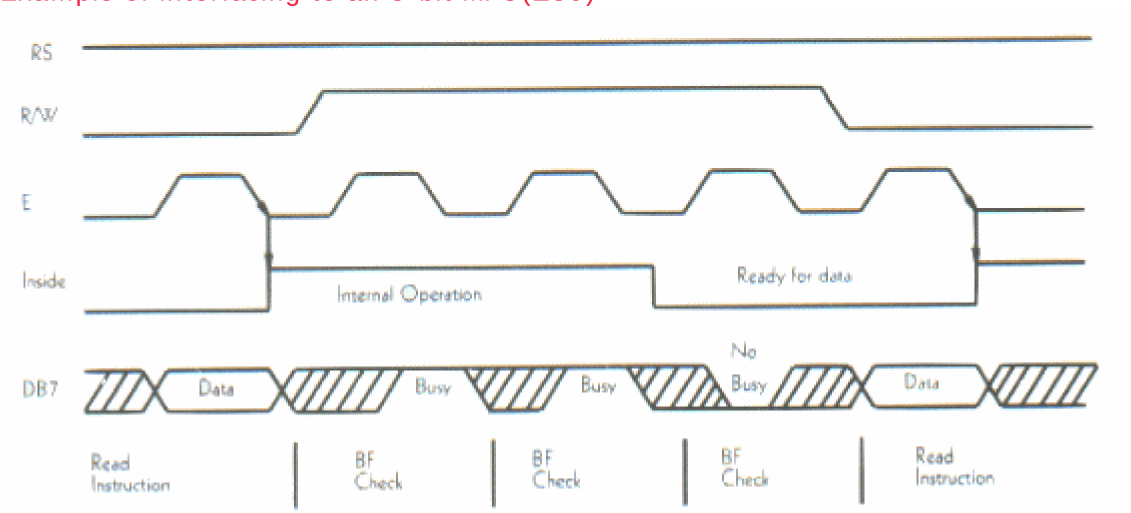
Technical

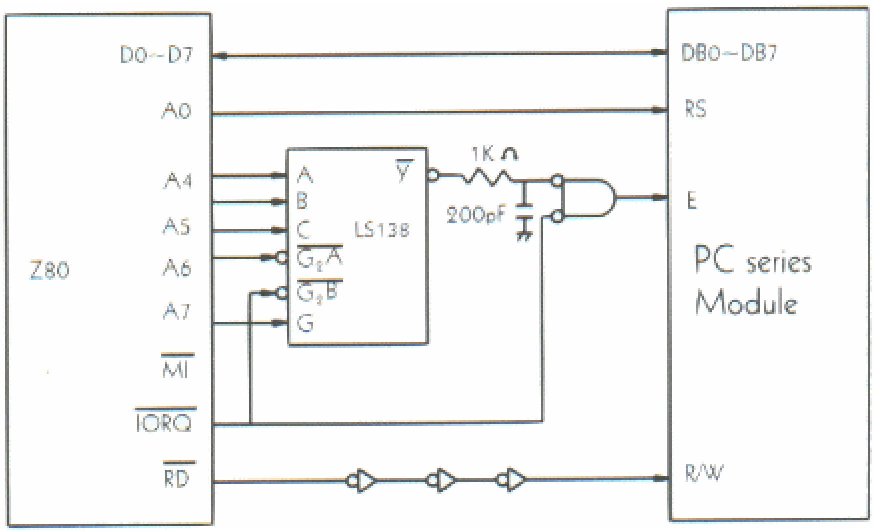
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Interface With MPU

- Example of interfacing to an 8-bit MPU(Z80)
- Example of interfacing to a 4-bit MPU
- If interface data is 4-bits long
- If interface data is 8-bits long

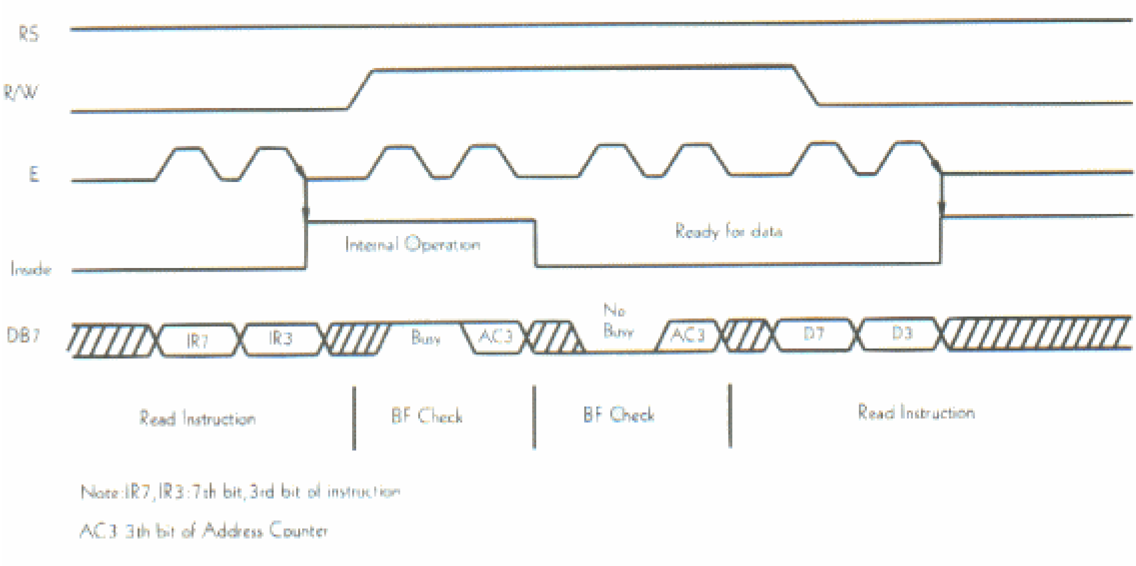
Example of interfacing to an 8-bit MPU(Z80)

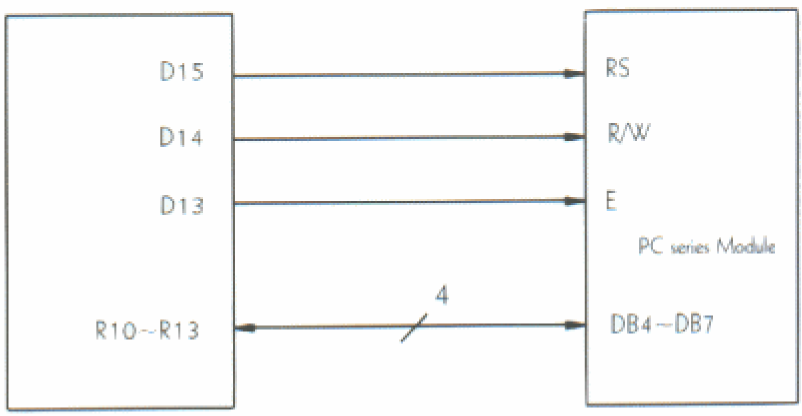




Example of interface to a 4-bit MPU

Interface to a 4-bit MPU can be made through the I/O port of the 4-bit MPU. If there are sufficient I/O ports, data can be transferred at 8-bit cycles, however, if there are not, data transfer can be accomplished by two cycles of 4-bit transfers (select interface as 4-bits long). Please take into account that 2 cycles of the BF check will be necessary and the timing sequence will prove to be complicated.





Features:

1. Interface to an 8-bit or 4-bit MPU is available.
2. 192 types of alphanumerics, symbols and special characters can be displayed with the multi built-in character generator(ROM).
3. Other preferred characters can be displayed by character generator(RAM)
4. Various instructions may be programmed.
   - Clear display
   - Cursor at home
   - On/Off cursor
   - Blink character
   - Shift display
   - Shift cursor
   - Read/write display data, etc.
5. Compact and light weight design which can easily be integrated into end products.
6. single power supply +5V drive(except for extended temp. type).
7. Low power consumption.
   - Interface between data bus line and 4-bit or 8-bit MPU is available.
   - Data transfer requires two cycles in case of a 4-bit MPU, and once in case of an 8-bit MPU.

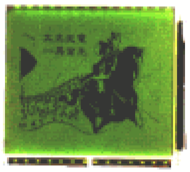
If Interface Data Is 4-bit long

- Data transfer is accomplished through 4 bus lines from DB4 to DB7.(while the rest of 4 bus lines from DB0 to DB3 are not used.)
- Data transfer is completed when 4-bits of data is transferred twice.(upper 4-bits of data, then lower 4-bits of data.)

If Interface Data Is 8-bits Long

- Data transfer is made through all 8 bus lines from DB0 to DB7.

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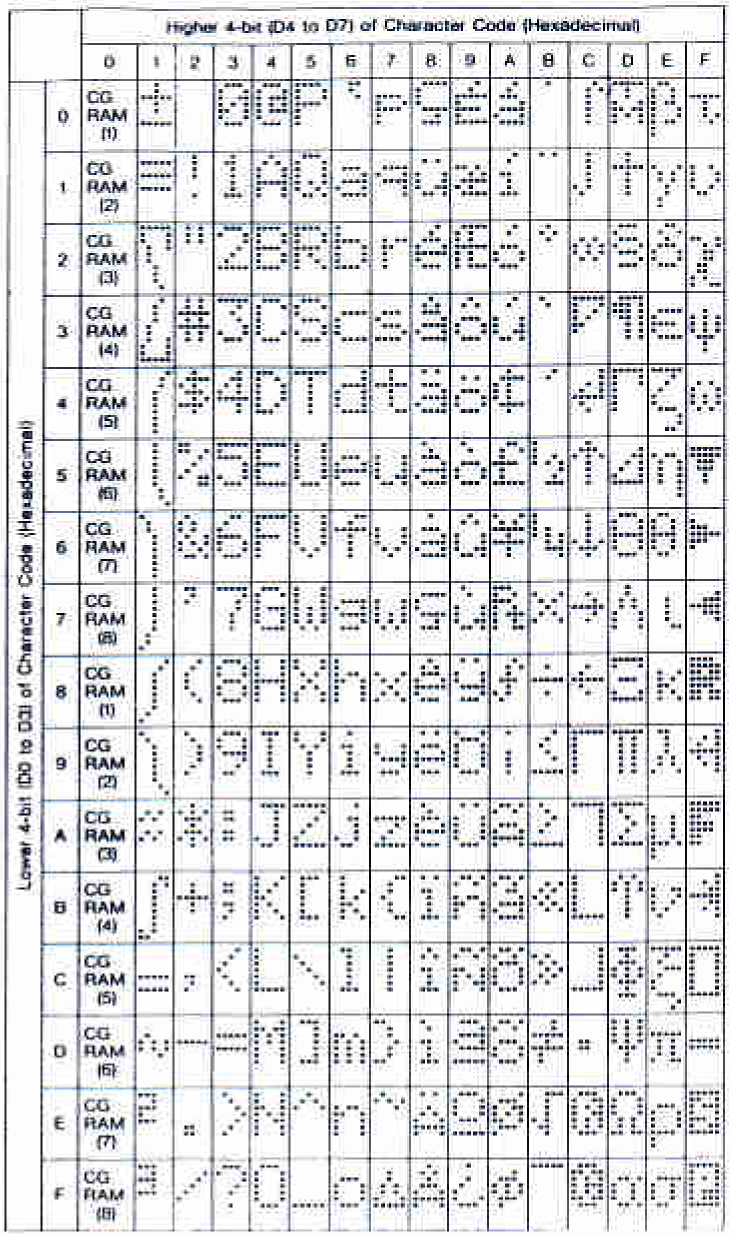
Technical

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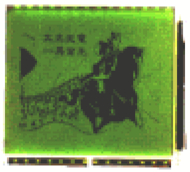
STOCKING DISTRIBUTOR SALES NETWORK CONTACT US

Standard Character Pattern

- Character Pattern (WB)
- Character Pattern (HC)
- Character Pattern (NI)
- Character Pattern (JA)
- Character Pattern (SO,WA)
- Character Pattern
- Character Pattern (N5)
- Character Pattern
- Character Pattern (N4)
- Character Pattern (TA)
- Character Pattern (NH)
- Character Pattern (YA)



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Technical

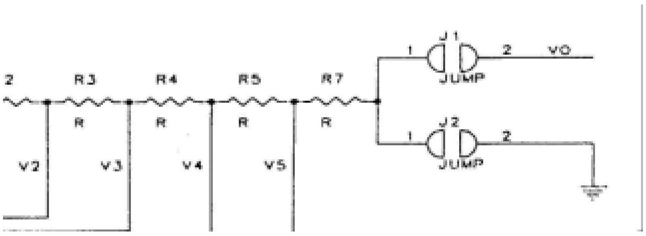
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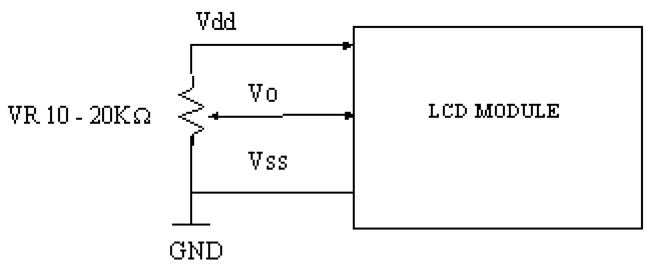
1. Adjusting the contrast of a character LCD module.

There are two means of adjusting the contrast: Please refer to the following drawing:

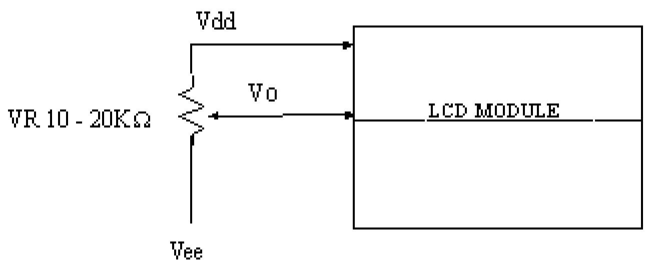


1. Internal: J2 short, add the appropriate resister to R7 for contrast control.
2. External: J1 short, R7=0, By adding a VR the contrast can be controlled externally. Please note the following diagram:

(1) Single Power Source

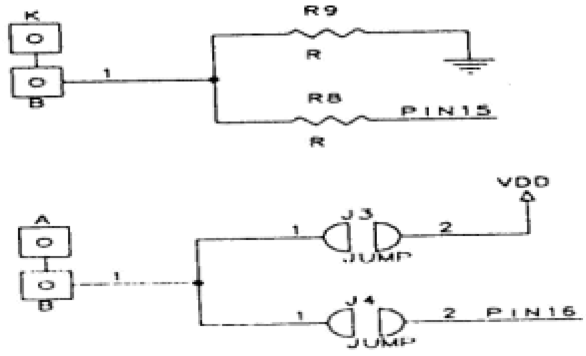


(2) Dual Power Source



2. Connecting and powering the backlight.

There are two means of connecting and powering the backlight. Please refer to the below diagrams:



1. PINS 1 & 2 (Vdd & Vss): J3 short, by adding a resistor on R9.
2. PINS 15 & 16: J4 short, by adding a resistor on R8.

NOTE: The brightness can be controlled by the value of R8 or R9.

3. Reference table for establishing the relationship between the temperature range, viewing direction and type of polarizer:

Polarizer	Normal		Extended		Normal		Extended	
	06:00	12:00	06:00	12:00	03:00	09:00	03:00	09:00
Reflective	A	D	G	J	M	P	S	V
Transflective	B	E	H	K	N	Q	T	W
Transmissive	C	F	I	L	O	R	U	X

4. Differences between a driver IC, a controller IC and a controller/driver IC:

Driver IC: There are two types of driver IC's. One is a "common" driver and the other a "segment" driver. Common drivers output signals to create the rows or number of lines while the segment drivers output the necessary signals to create the characters or columns.

Controller IC: This IC receives data written in ASCII or JIS code from the MPU and stores this data in RAM. This data is then converted into a serial character pattern and transferred to the LCD driver IC.

Driver/Controller IC: It is most commonly found in a graphics module. It receives data from the MPU and stores it in RAM. It accepts commands directly from the MPU for both the common and segment drivers.

5. Following is the minimum dot size and pitch on the LCD, the ITO line on the LCD and the elastomer (zebra) connector:

ITEM	Dots or Lines	Gaps
LCD Dots	0.22mm	0.02mm
LCD ITO lines	S=0.075, C=0.08mm	0.03mm
Rubber Connectors	0.025mm	0.025mm
Heat Seal	0.09mm	0.09mm

6. Advantages and disadvantages of backlight versions:

ITEM	LED	EL	CCFL
Type	Edge & Array	Thin Flat Panel	Direct & edge lighting
Power Requirement	DC4.2V, High power consumption in array type	AC110~130V, 400HZ need DC/AC converter , Low power consumption	AC600~1000V, 30KHZ, Need DC/AC converter, Low power consumption
Brightness	15 ~ 80CD/M^2	70 ~ 200CD/M^2	200 ~ 600CD/M^2
Life	50,000 ~ 100,000hr	2,000 ~5,000hr	10,000 ~ 20,000hr
Thickness	Array: 5mm, Edge: 1.3 ~ 4mm	1.5mm Max	Direct: 15.0mm Edge: 3.0mm
Color	Yellow/Green, Amber, Red, Orange, Green	Blue/Green, White, Yellow/Green	White

7. Comparison between TN, STN and FSTN technologies:

ITEM	Contrast Ratio	View Angle	COST
TN	3	3	3
STN	2	2	2
FSTN	1	1	1

Remarks: with 1 being the best or most expensive and 3 the worst or least expensive.

8. Differences between reflective, transflective and transmissive displays

Reflective: Such display includes a diffuser. This layer reflects the light that enters the front of the display. Reflective displays require ambient light for the light source since there is no backlight.

Transflective: As type of backing which is bonded to the rear polarizer. Enables light to pass through the back, as well as reflecting light from the front.

Transmissive: A type of LCD which does not have a reflector or transflector laminated to the rear polarizer. A backlight must be used with this type of LCD configuration. The most common is a transmissive negative image.

9. Considerations for attaining a 3.0 Volt LCD module:

IC: Choose the ICs that can be driven at 3.3V or less. Below is a list of IC's that can accomplish this requirement:

Controller:

KS0066U 2.7 ~ 5.5V

KS0070B 2.7 ~ 5.5V

HD44780U 2.7 ~ 5.5V

Driver:

KS0065 2.7 ~ 5.5V

KS0063 2.7 ~ 5.5V

SED1181 5.0V min.

LCD panel: The driving voltage for most all LCD panels is above 3.3V. It is necessary to then add a "negative voltage" IC on the PCB of the module or to the customer's motherboard to raise the voltage. A couple of NV generators is as follows:

NV IC: SCI7661 3X with temperature compensation.

SCI7660 2X, dice font available (at a much less expensive cost).

If a NV IC must be incorporated onto the module PCB, there is apt to be two possible considerations:

1. Tooling cost
2. The PCB is too small to accommodate the NV IC. If there is not sufficient space, a possible solution would be to replace one controller with a driver, with single controller (such as replacing a KS0066(U) & KS0065(B) with a KS0070). The per unit cost will be a little greater but it will save overall space on the PCB and eliminate having to re-tool the PCB.

- Some TAB IC's such as SED1560 series include a power circuit, which can amplify the input voltage to drive the LCD. In this case it is not necessary to add a NV IC to raise the voltage.

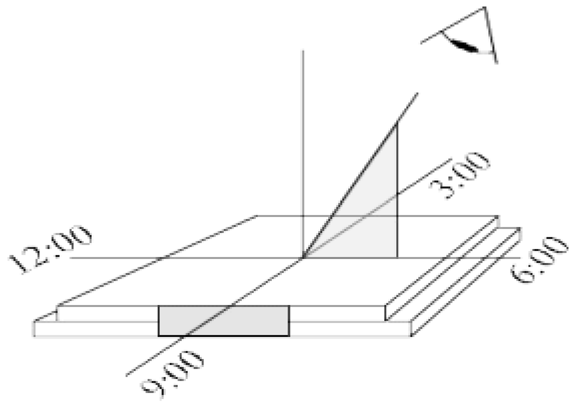
C. Backlight:

CCFL & EL: These backlight options require an inverter. The inverter chosen cannot exceed 3.3 Volts.

LED: In an attempt to achieve this 3.3V requirement it is necessary to use an edge-lit LED. Note this edge-lit LED will still consume a large current.

10. Reference to Viewing angle:

Viewing Angle is the direction by which the display will look best. This is established during the manufacturing process and can not be changed by rotating the polarizer. Viewing direction is specified in terms of a clock position, such as 6:00 & 12:00. Please refer to the following drawing:



11. Clarification to the term "rainbow" effect:

This refers to a red and green circle or rainbow on the LCD glass. The LCD panel under uneven pressure causes this problem from the bezel. It is very common in LCD modules and normally it will not affect the performance or the appearance of the display when operational.

12. Pin assignments for a Character module:

Example of a standard 14-pin character module:

PIN 1: Vss

PIN 2: Vdd

PIN 3: Vo

PIN 4: RS

PIN 5: R/W

PIN 6: Enable

PIN 7 ~ 14: DB0 ~ DB7

13. What is temperature compensation and why is required

A LCD operating voltage varies at different temperatures. The operating voltage must rise as temperature lowers or the contrast will degrade. Conversely, the operating temperature must fall as the temperature rises or the contrast will degrade. For this reason it is often a requirement, with graphics modules, to control the input voltage accordingly. The temperature compensation circuit is the circuit that controls the input voltage as the temperature changes. This temperature compensation circuit can be located on the LCD module or on the customer's motherboard.

14. Troubleshooting a LED backlit module in which the display is turning dark:

This problem is more than likely caused by the temperature rise from the LED backlight. In this case the LED backlight has consumed too much of the power. When the temperature rises, the V_{LCD} becomes lower causing the input voltage to be too high. The result is a poor contrast and the display becoming too dark. The solution would be to lower the power consumption of the LED. This can be accomplished by raising the value of R8 or R9 to reduce the current to the LED backlight.

15. How to control the LED backlight on a 14-pin module:

Short J2, the Vdd is controlling the input to the LED backlight. In addition, it is necessary to place a current limiting resistor to lower the voltage from 5V to 4.2V.

Note: If the LED is drawing too much current, it may cause the Vdd † Vo too low and the contrast becomes poor. If this should occur increasing the value of R9 should decrease the current draw to the LED backlight or another approach would be to increase the voltage input to the LCD by decreasing the value of R7.

16. Examples of the current consumption of an LED backlit, EL backlit and the LCD for the following modules:

Products	LCM	LED	EL
PC1602-F	1.3mA	120mA	3.26mA
PC2002-B	1.8mA	200mA	5.3mA
PC2004-A	1.8mA	260mA	7.2mA
PC4004-A	2.2mA	440mA	7.5mA

17. Following is the Vop range for a Character and Graphics LCD module:

LCD Type	Vop for N.T.	Vop for W.T.
Character	4.2 ~ 4.8V	5 ~ 9V
Graphic	5.5 ~ 26V	6 ~ 28V

Note: N.T. = normal temperature

W.T.= wide temperature

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Sitronix

ST7066U

Dot Matrix LCD Controller/Driver

■ Features

- **5 x 8 and 5 x 11 dot matrix possible**
- **Low power operation support:**
- **-- 2.7 to 5.5V**
- **Wide range of LCD driver power**
  -- 3.0 to 10V
- **Correspond to high speed MPU bus interface**
  -- 2 MHz (when V_{CC} = 5V)
- **4-bit or 8-bit MPU interface enabled**
- **80 x 8-bit display RAM (80 characters max.)**
- **13,200-bit character generator ROM for a total of 240 character fonts(5 x 8 dot or 5 x 11 dot)**
- **64 x 8-bit character generator RAM**
  -- 8 character fonts (5 x 8 dot)
  -- 4 character fonts (5 x 11 dot)
- **16-common x 40-segment liquid crystal display driver**
- **Programmable duty cycles**
  -- 1/8 for one line of 5 x 8 dots with cursor
  -- 1/11 for one line of 5 x 11 dots & cursor
  -- 1/16 for two lines of 5 x 8 dots & cursor
- **Wide range of instruction functions:**
  Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- **Pin function compatibility with HD44780, KS0066 and SED1278**
- **Automatic reset circuit that initializes the controller/driver after power on**
- **Internal oscillator with external resistors**
- **Low power consumption**
- **QFP80 and Bare Chip available**

■ Description

The ST7066U dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

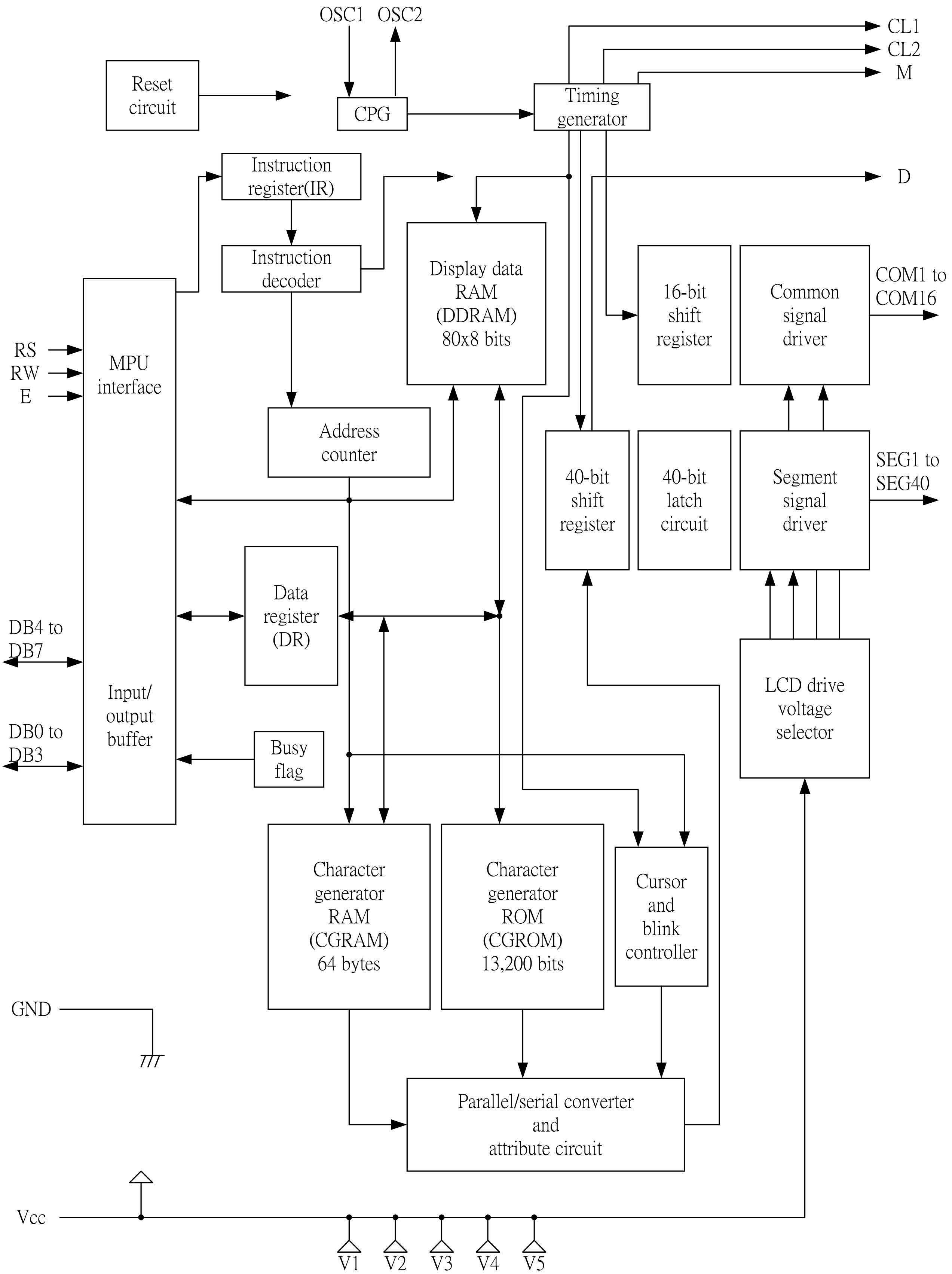
The ST7066U has pin function compatibility with the HD44780, KS0066 and SED1278 that allows the user to easily replace it with an ST7066U. The ST7066U character generator ROM is extended to generate 240 5x8(5x11) dot character fonts for a total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the ST7066U is suitable for any portable battery-driven product requiring low power dissipation.

The ST7066U LCD driver consists of 16 common signal drivers and 40 segment signal drivers which can extend display size by cascading segment driver ST7065 or ST7063. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7066U can display up to one 8-character line or two 8-character lines.

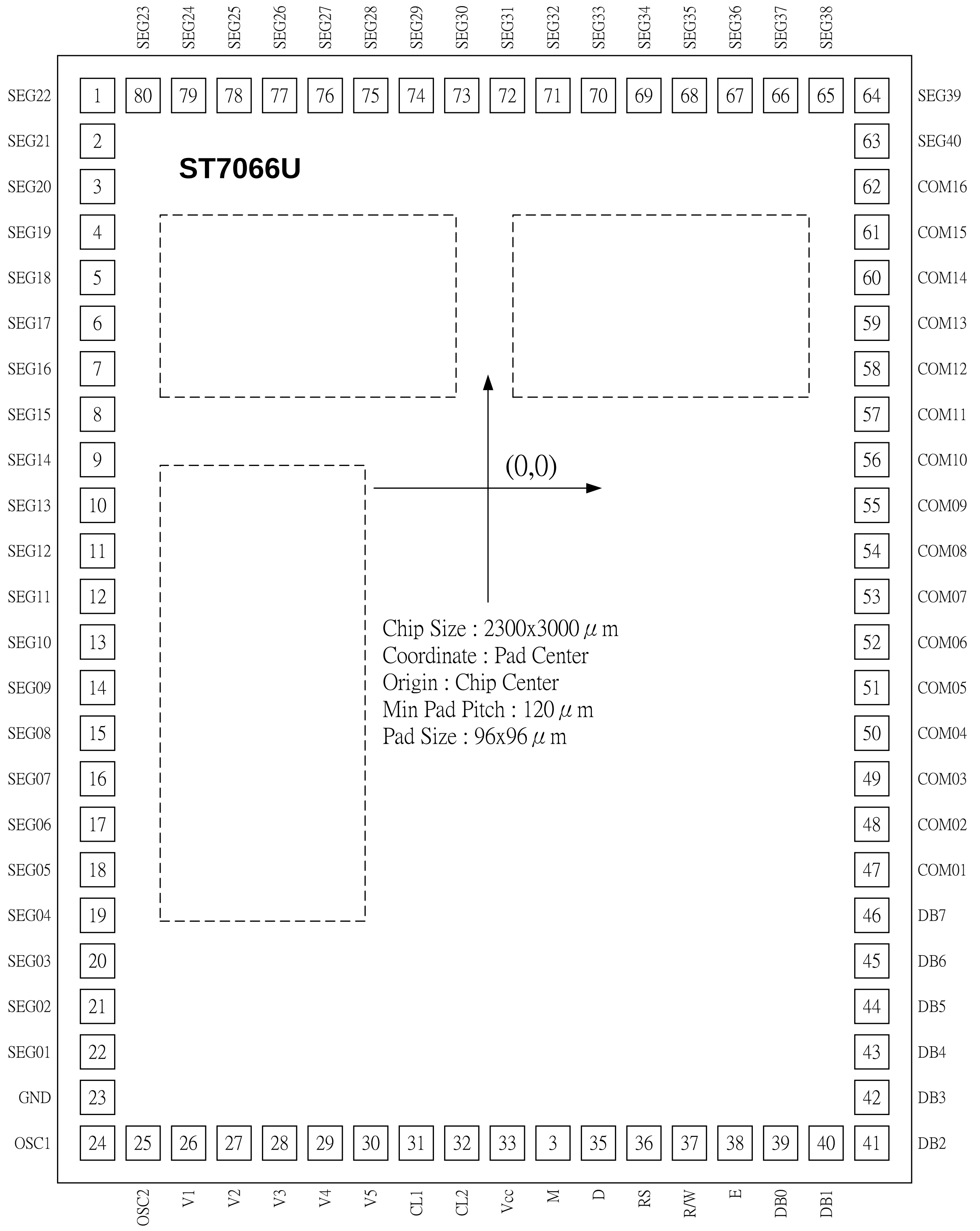
Product Name	Support Character
ST7066U-0A	English / Japan
ST7066U-0B	English / European
ST7066U-0E	English / European

ST7066 Serial Specification Revision History		
Version	**Date**	**Description**
1.7	2000/10/31	1. Added 8051 Example Program Code(Page 21,23) 2. Added Annotated Flow Chart : "BF cannot be checked before this instruction" 3. Changed Maximum Ratings Power Supply Voltage:+5.5V →+7.0V(Page 28)
1.8	2000/11/14	Added QFP Pad Configuration(Page 5)
1.8a	2000/11/30	1. Moved QFP Package Dimensions(Page 39) to Page 5 2. Changed DC Characteristics Ratings(Page 32,33)
2.0	2001/03/01	Transition to ST7066U

■ Block Diagram



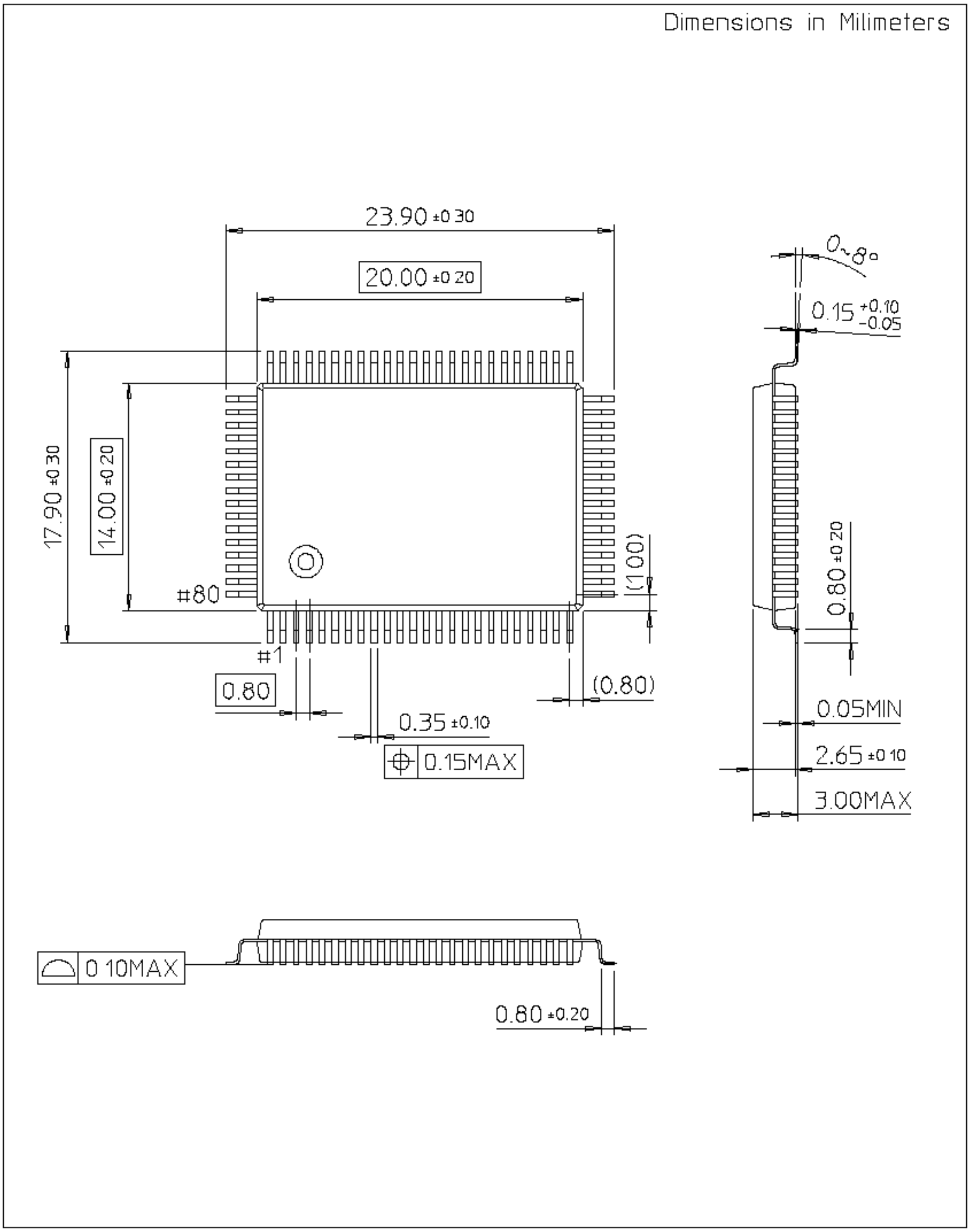
■ Pad Arrangement



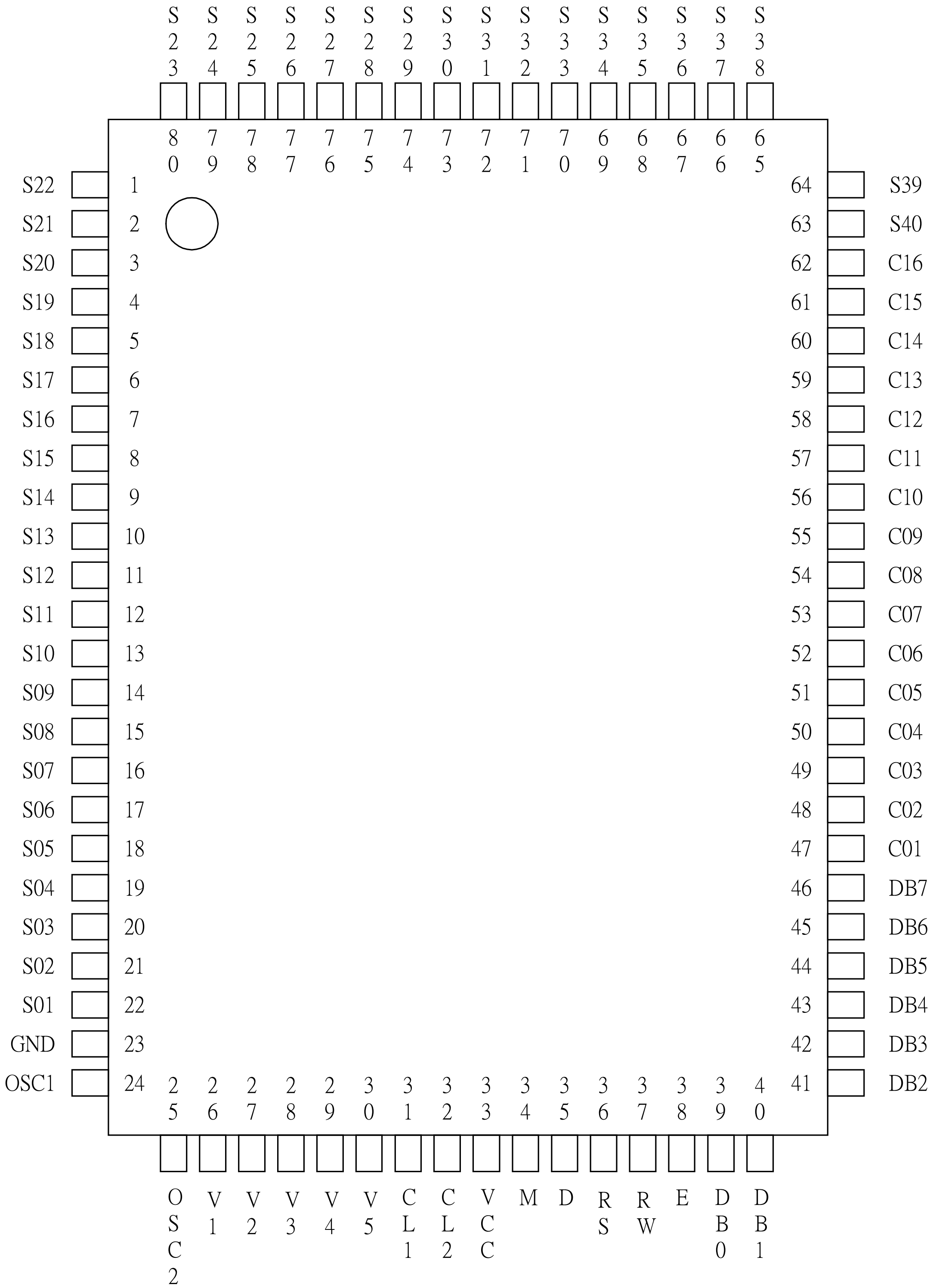
Substrate Connect to VDD.

■ Package Dimensions

80-QFP-1420C



■ Pad Configuration(80 QFP)



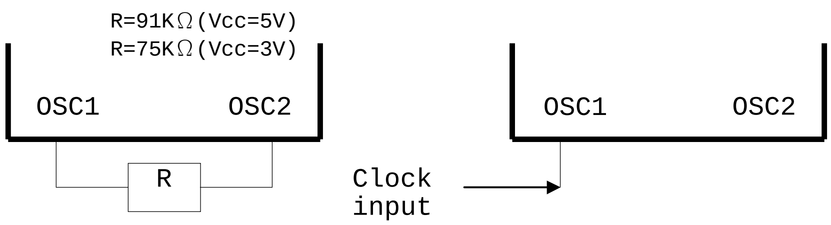
■ Pad Location Coordinates

Pad No.	Function	X	Y
1	SEG22	-1040	1400
2	SEG21	-1040	1270
3	SEG20	-1040	1140
4	SEG19	-1040	1020
5	SEG18	-1040	900
6	SEG17	-1040	780
7	SEG16	-1040	660
8	SEG15	-1040	540
9	SEG14	-1040	420
10	SEG13	-1040	300
11	SEG12	-1040	180
12	SEG11	-1040	60
13	SEG10	-1040	-60
14	SEG9	-1040	-180
15	SEG8	-1040	-300
16	SEG7	-1040	-420
17	SEG6	-1040	-540
18	SEG5	-1040	-660
19	SEG4	-1040	-780
20	SEG3	-1040	-900
21	SEG2	-1040	-1020
22	SEG1	-1040	-1140
23	GND	-1040	-1270
24	OSC1	-1040	-1400
25	OSC2	-910	-1400
26	V1	-780	-1400
27	V2	-660	-1400
28	V3	-540	-1400
29	V4	-420	-1400
30	V5	-300	-1400
31	CL1	-180	-1400
32	CL2	-60	-1400
33	Vcc	60	-1400
34	M	180	-1400
35	D	300	-1400
36	RS	420	-1400
37	RW	540	-1400
38	E	660	-1400
39	DB0	780	-1400
40	DB1	910	-1400
41	DB2	1040	-1400
42	DB3	1040	-1270
43	DB4	1040	-1140
44	DB5	1040	-1020
45	DB6	1040	-900
46	DB7	1040	-780
47	COM1	1040	-660
48	COM2	1040	-540
49	COM3	1040	-420
50	COM4	1040	-300
51	COM5	1040	-180
52	COM6	1040	-60
53	COM7	1040	60
54	COM8	1040	180
55	COM9	1040	300
56	COM10	1040	420
57	COM11	1040	540
58	COM12	1040	660
59	COM13	1040	780
60	COM14	1040	900
61	COM15	1040	1020
62	COM16	1040	1140
63	SEG40	1040	1270
64	SEG39	1040	1400
65	SEG38	910	1400
66	SEG37	780	1400
67	SEG36	660	1400
68	SEG35	540	1400
69	SEG34	420	1400
70	SEG33	300	1400
71	SEG32	180	1400
72	SEG31	60	1400
73	SEG30	-60	1400
74	SEG29	-180	1400
75	SEG28	-300	1400
76	SEG27	-420	1400
77	SEG26	-540	1400
78	SEG25	-660	1400
79	SEG24	-780	1400
80	SEG23	-910	1400

■ Pin Function

Name	Number	I/O	Interfaced with	Function
RS	1	I	MPU	Select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/W	1	I	MPU	Select read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write.
DB4 to DB7	4	I/O	MPU	Four high order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. DB7 can be used as a busy flag.
DB0 to DB3	4	I/O	MPU	Four low order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. These pins are not used during 4-bit operation.
CL1	1	O	Extension driver	Clock to latch serial data D sent to the extension driver
CL2	1	O	Extension driver	Clock to shift serial data D
M	1	O	Extension driver	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	Extension driver	Character pattern data corresponding to each segment signal
COM1 to COM16	16	O	LCD	Common signals that are not used are changed to non-selection waveform. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor.
SEG1 to SEG40	40	O	LCD	Segment signals
V1 to V5	5	-	Power supply	Power supply for LCD drive V_{CC} - V5 = 10 V (Max)
V_{CC}, GND	2	-	Power supply	V_{CC}: 2.7V to 5.5V, GND: 0V
OSC1, OSC2	2		Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.

Note:
1. Vcc>=V1>=V2>=V3>=V4>=V5 must be maintained
2. Two clock options:



Function Description

System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Table 1. Various kinds of operations according to RS and R/W bits.

Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

● Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

➢ 1-line display (N = 0) (Figure 2)

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the ST7066U, 8 characters are displayed. See Figure 3.
When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

	High Order bits			Low Order bits			
AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example: DDRAM Address 4F

1	0	0	1	1	1	1

Figure 1 DDRAM Address

Display Position (Digit)	1	2	3	4	5	6		78	79	80
DDRAM Address	00	01	02	03	04	05	……………….	4D	4E	4F

Figure 2 1-Line Display

Display Position	1	2	3	4	5	6	7	8
DDRAM Address	00	01	02	03	04	05	06	07
For Shift Left	01	02	03	04	05	06	07	08
For Shift Right	4F	00	01	02	03	04	05	06

Figure 3 1-Line by 8-Character Display Example

➢ 2-line display (N = 1) (Figure 4)

Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the ST7066U is used, 8 characters × 2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

Display Position	1	2	3	4	5	6		38	39	40
DDRAM Address (hexadecimal)	00	01	02	03	04	05	……………….	25	26	27
	40	41	42	43	44	45	……………….	65	66	67

Figure 4 2-Line Display

Display Position	1	2	3	4	5	6	7	8
DDRAM Address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For Shift Left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For Shift Right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 5 2-Line by 8-Character Display Example

Case 2: For a 16-character × 2-line display, the ST7066U can be extended using one 40-output extension driver. See Figure 6.
When display shift operation is performed, the DDRAM address shifts. See Figure 6.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
For Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 6 2-Line by 16-Character Display Example

- **Character Generator ROM (CGROM)**

The character generator ROM generates 5 x 8 dot or 5 x 11 dot character patterns from 8-bit character codes. It can generate 240 5 x 8 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

- **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 11 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

- **Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

- **LCD Driver Circuit**

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch. In case of 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have 1/11duty , and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

- **Cursor/Blink Control Circuit**

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: 0A)



Table 4(Cont.) (ROM Code: 0B)

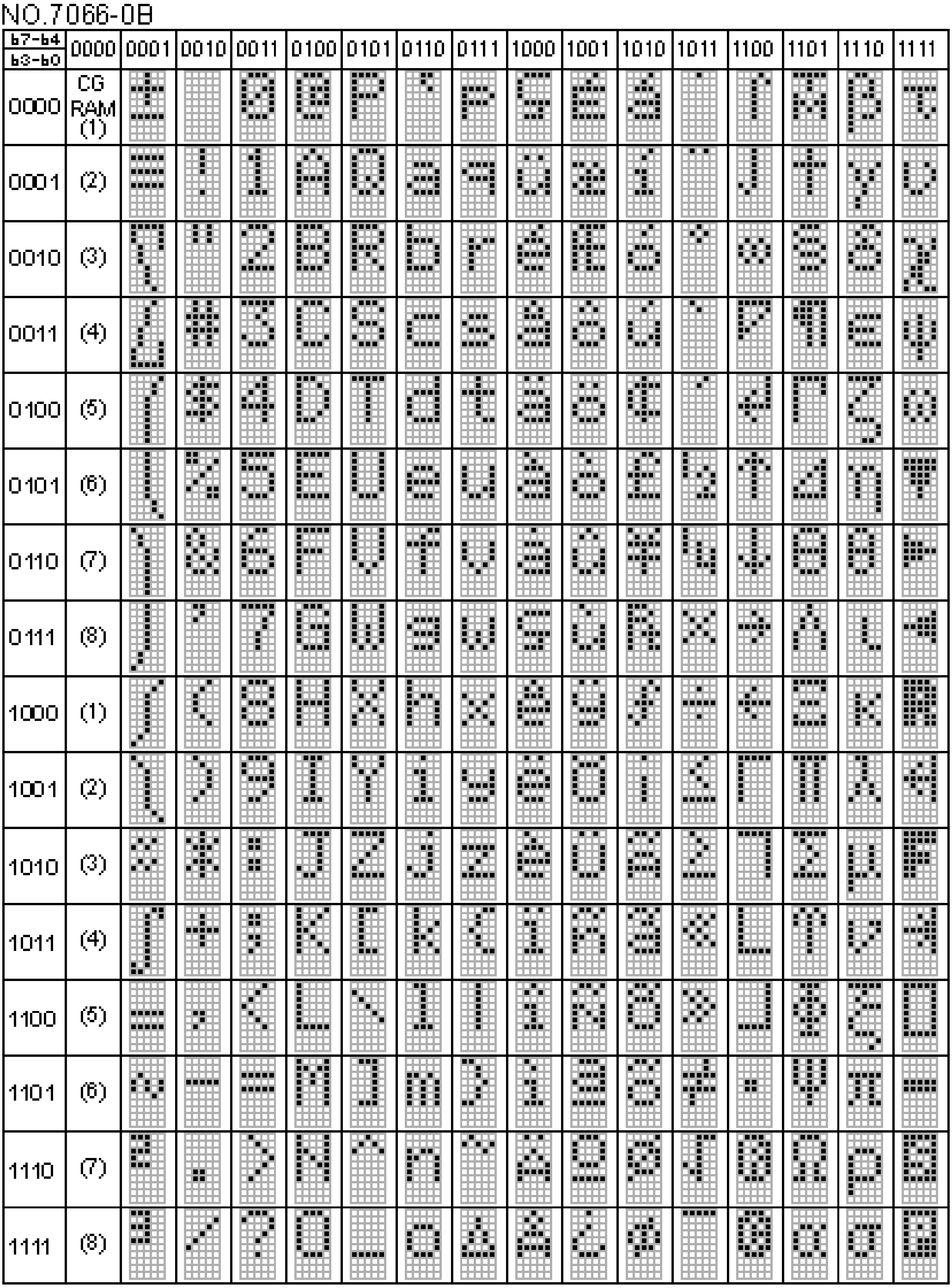
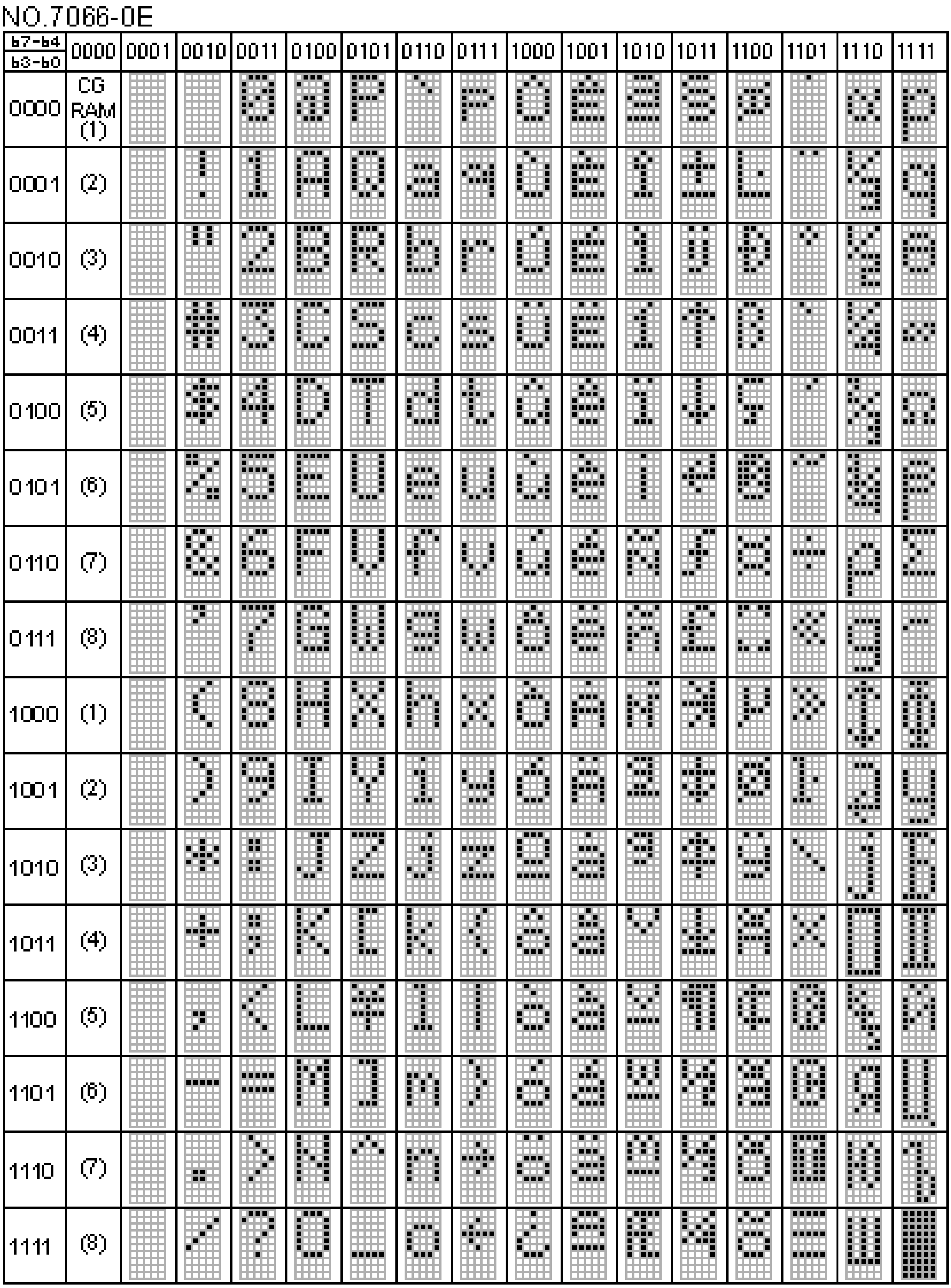


Table 4(Cont.) (ROM Code: 0E)



Character Code (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
					0	0	0				0	0	0				1	1	1	1	1
					0	0	0				0	0	1				0	0	1	0	0
					0	0	0				0	1	0				0	0	1	0	0
0	0	0	0	-	0	0	0	0	0	0	0	1	1	-	-	-	0	0	1	0	0
					0	0	0				1	0	0				0	0	1	0	0
					0	0	0				1	0	1				0	0	1	0	0
					0	0	0				1	1	0				0	0	1	0	0
					0	0	0				1	1	1				0	0	0	0	0
					0	0	1				0	0	0				1	1	1	1	0
					0	0	1				0	0	1				1	0	0	0	1
					0	0	1				0	1	0				1	0	0	0	1
0	0	0	0	-	0	0	1	0	0	1	0	1	1	-	-	-	1	1	1	1	0
					0	0	1				1	0	0				1	0	1	0	0
					0	0	1				1	0	1				1	0	0	1	0
					0	0	1				1	1	0				1	0	0	0	1
					0	0	1				1	1	1				0	0	0	0	0

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
"-": Indicates no effect.

■ Instructions

There are four categories of instructions that:

- **Designate ST7066U functions, such as display format, data length, etc.**
- **Set internal RAM addresses**
- **Perform data transfer with internal RAM**
- **Others**

Instruction Table:

Instruction	Instruction Code										Description	Description Time (270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	37 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 us
Function Set	0	0	0	0	1	DL	N	F	x	x	DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8	37 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	37 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	37 us

Note:
Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

■ Instruction Description

- **Clear Display**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

- **Entry Mode Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

➢ **I/D : Increment / decrement of DDRAM address (cursor or blink)**

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

➢ **S: Shift of entire display**

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Display ON/OFF**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
  When D = "High", entire display is turned on.
  When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
  When C = "High", cursor is turned on.
  When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
  When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
  When B = "Low", blink is off.

- **Cursor or Display Shift**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	x	x

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	x	x

- **DL : Interface data length control bit**

  When DL = "High", it means 8-bit bus mode with MPU.

  When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

  When 4-bit bus mode, it needs to transfer 4-bit data by two times.

- **N : Display line number control bit**

  When N = "Low", it means 1-line display mode.

  When N = "High", 2-line display mode is set.

- **F : Display font type control bit**

  When F = "Low", it means 5 x 8 dots format display mode

  When F = "High", 5 x11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5x8	1/8
L	H	1	5x11	1/11
H	x	2	5x8	1/16

- **Set CGRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

- **Read Busy Flag and Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = "High", indicates that the internal operation is being processed.So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

■ Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the ST7066U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5x8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note:
If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the ST7066U. For such a case, initialization must be performed by the MPU as explain by the following figure.

■ Initializing by Instruction

- **8-bit Interface (fosc=270KHz)**

POWER ON

↓

Wait time >40mS
After Vcc >4.5V

↓

Function set ← BF cannot be checked before this instruction.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	X	X

↓

Wait time >37uS

↓

Function set ← BF cannot be checked before this instruction.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	X	X

↓

Wait time >37uS

↓

Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

↓

Wait time >37uS

↓

Display clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

↓

Wait time >1.52mS

↓

Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

↓

Initialization end

- **Initial Program Code Example For 8051 MPU(8 Bit Interface):**

```
;-------------------------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK        ;CURSOR MOVES TO RIGHT
        CALL    DELAY37uS
;-------------------------------------------------------------------------------
MAIN_START:

        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
;-------------------------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        CLR     RS                      ;EX:Port 3.0
        CLR     RW                      ;EX:Port 3.1
        SETB    E                       ;EX:Port 3.2
        MOV     P1,A                    ;EX:Port 1=Data Bus
        CLR     E
        MOV     P1,#FFH                 ;For Check Busy Flag
        RET
;-------------------------------------------------------------------------------
CHK_BUSY:                               ;Check Busy Flag
        CLR     RS
        SETB    RW
        SETB    E
        JB      P1.7,$
        CLR     E
        RET
```

- **4-bit Interface (fosc=270KHz)**

POWER ON

↓

Wait time >40mS
After Vcc >4.5V

↓

Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X

BF cannot be checked before this instruction.

↓

Wait time >37uS

↓

Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

BF cannot be checked before this instruction.

↓

Wait time >37uS

↓

Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

BF cannot be checked before this instruction.

↓

Wait time >37uS

↓

Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

↓

Wait time >37uS

↓

Display clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

↓

Wait time >1.52mS

↓

Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	S	X	X	X	X

↓

Initialization end

- **Initial Program Code Example For 8051 MPU(4 Bit Interface):**

```
;-----------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK
        CALL    DELAY37uS
;-----------------------------------------------------------------
MAIN_START:
        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
```

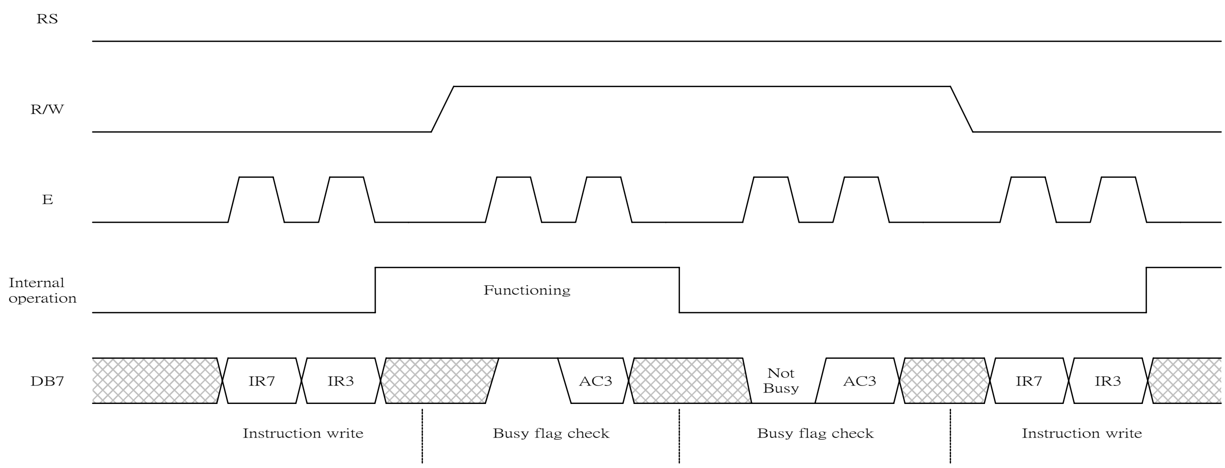
```
;-----------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        PUSH    A
        ANL     A,#F0H
        CLR     RS              ;EX:Port 3.0
        CLR     RW              ;EX:Port 3.1
        SETB    E               ;EX:Port 3.2
        MOV     P1,A            ;EX:Port1=Data Bus
        CLR     E
        POP     A
        SWAP    A
WRINS_ONCE:
        ANL     A,#F0H
        CLR     RS
        CLR     RW
        SETB    E
        MOV     P1,A
        CLR     E
        MOV     P1,#FFH         ;For Check Bus Flag
        RET
;-----------------------------------------------------------------
CHK_BUSY:                       ;Check Busy Flag
        PUSH    A
        MOV     P1,#FFH
$1
        CLR     RS
        SETB    RW
        SETB    E
        MOV     A,P1
        CLR     E
        MOV     P1,#FFH
        CLR     RS
        SETB    RW
        SETB    E
        NOP
        CLR     E
        JB      A.7,$1
        POP     A
        RET
```

■ Interfacing to the MPU

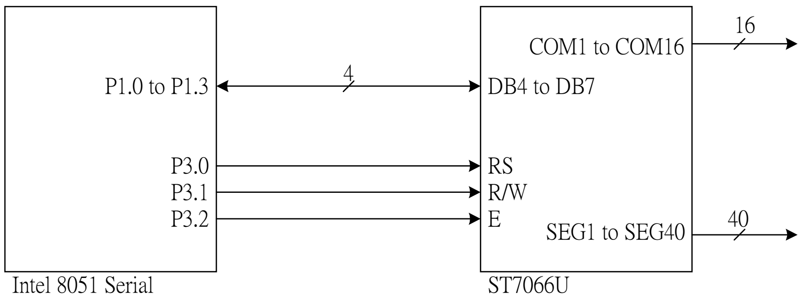
The ST7066U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPU.

- **For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.** Bus lines DB0 to DB3 are disabled. The data transfer between the ST7066U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

➢ **Example of busy flag check timing sequence**

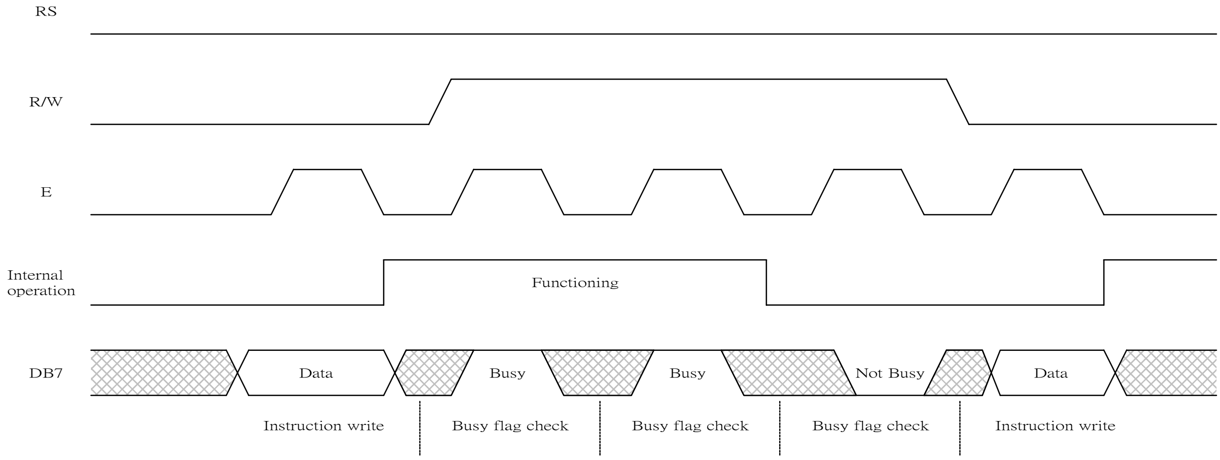


➢ **Intel 8051 interface**

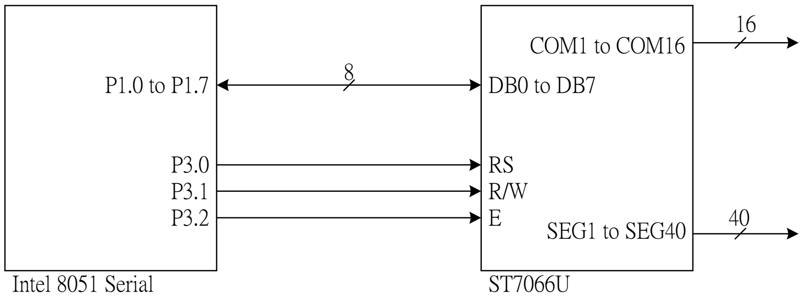


- **For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.**

➢ **Example of busy flag check timing sequence**



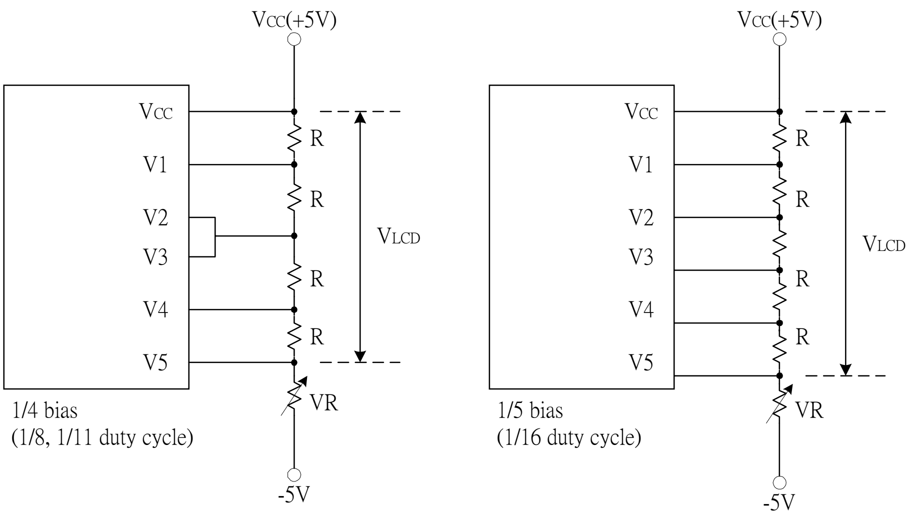
➢ **Intel 8051 interface**



■ Supply Voltage for LCD Drive

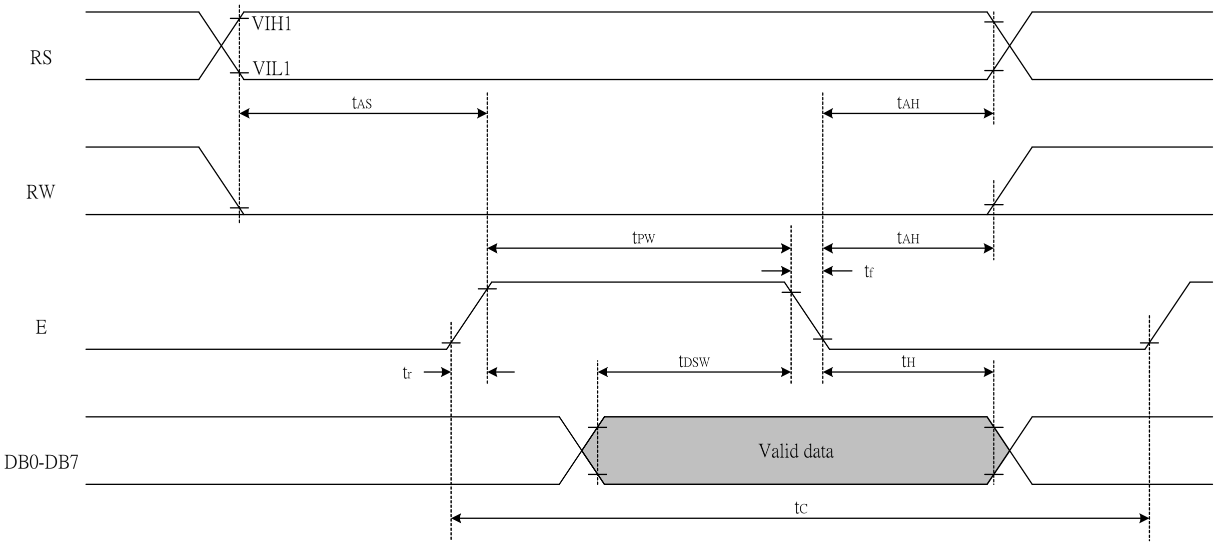
There are different voltages that supply to ST7066U's pin (V1 - V5) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Supply Voltage	1/4	1/5
V1	Vcc - 1/4VLCD	Vcc - 1/5VLCD
V2	Vcc - 1/2VLCD	Vcc - 2/5VLCD
V3	Vcc - 1/2VLCD	Vcc - 3/5VLCD
V4	Vcc - 3/4VLCD	Vcc - 4/5VLCD
V5	Vcc - VLCD	Vcc- VLCD

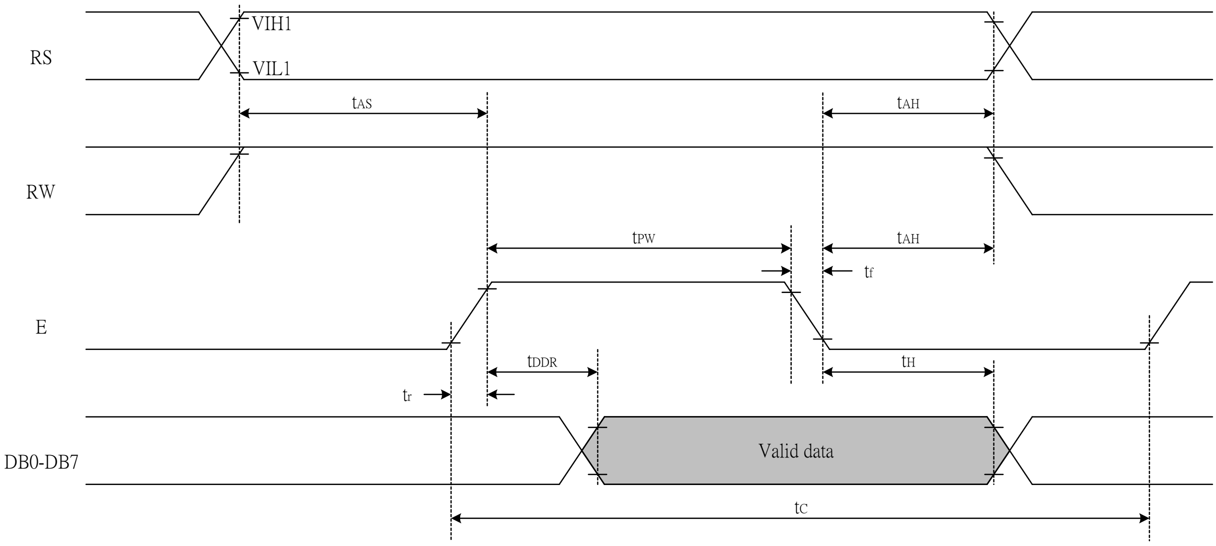


■ Timing Characteristics

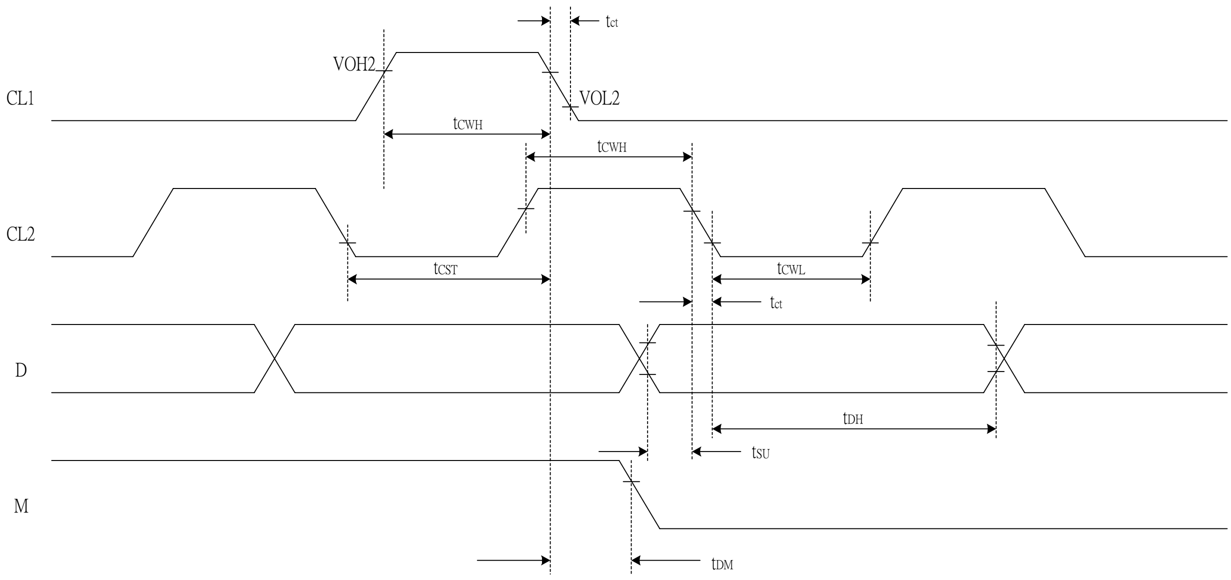
- **Writing data from MPU to ST7066U**



- **Reading data from ST7066U to MPU**



- **Interface Timing with External Driver**



■ AC Characteristics

(TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 75KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7066U)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	460	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	80	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from ST7066U to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	480	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	320	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver(ST7065)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

■ AC Characteristics

(TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7066U)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from ST7066U to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver(ST7065)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

■ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{CC}	-0.3 to +7.0
LCD Driver Voltage	V_{LCD}	Vcc-10.0 to Vcc+0.3
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3
Operating Temperature	T_A	-40°C to + 90°C
Storage Temperature	T_{STO}	-55°C to + 125°C

■ DC Characteristics

(TA = 25℃ , VCC = 2.7 V – 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V_{CC}-V5	3.0	-	10.0	V
I_{CC}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=3.0V	-	0.1	0.25	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2Vcc	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.75 Vcc	-	-	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.2Vcc	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	V_{CC} = 3V	-10	-50	-120	μA

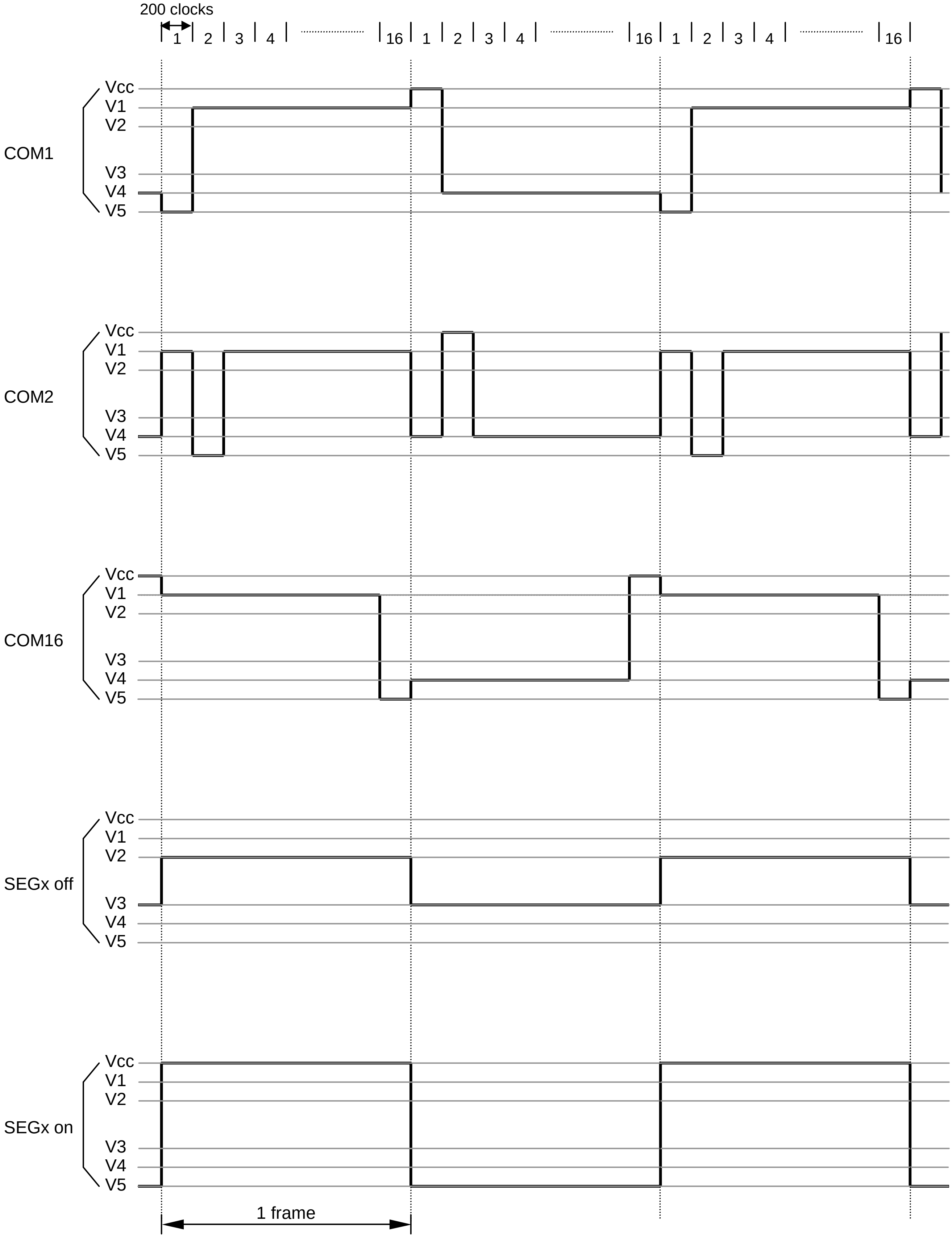
■ DC Characteristics

(TA = 25℃, V_{CC} = 4.5 V - 5.5 V)

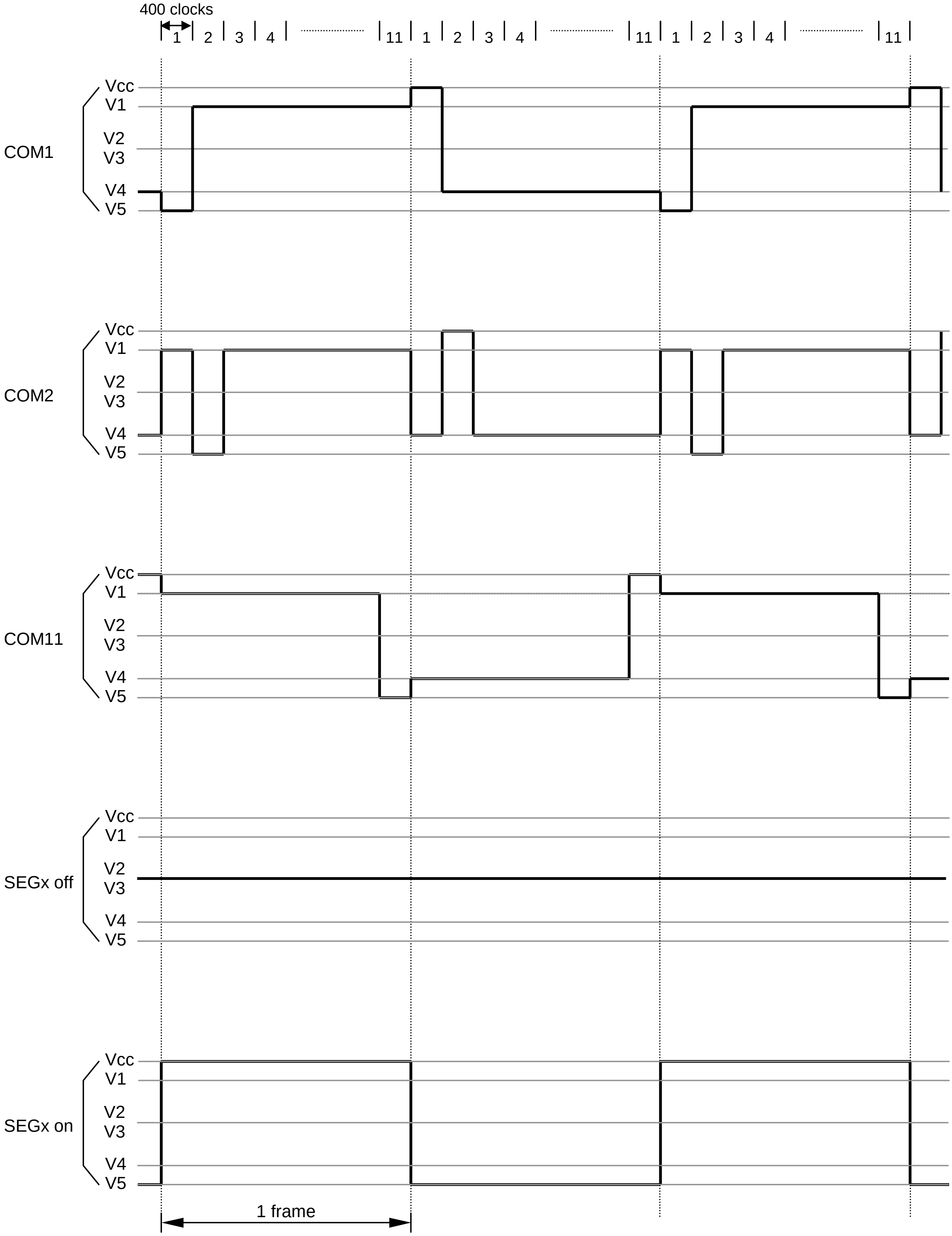
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V_{CC}-V5	3.0	-	10.0	V
I_{CC}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=5.0V	-	0.2	0.5	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{CC}-1	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	3.9	-	V_{CC}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.4	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.9V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.1V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{CC} = 5V	-50	-110	-180	µA

■ LCD Frame Frequency

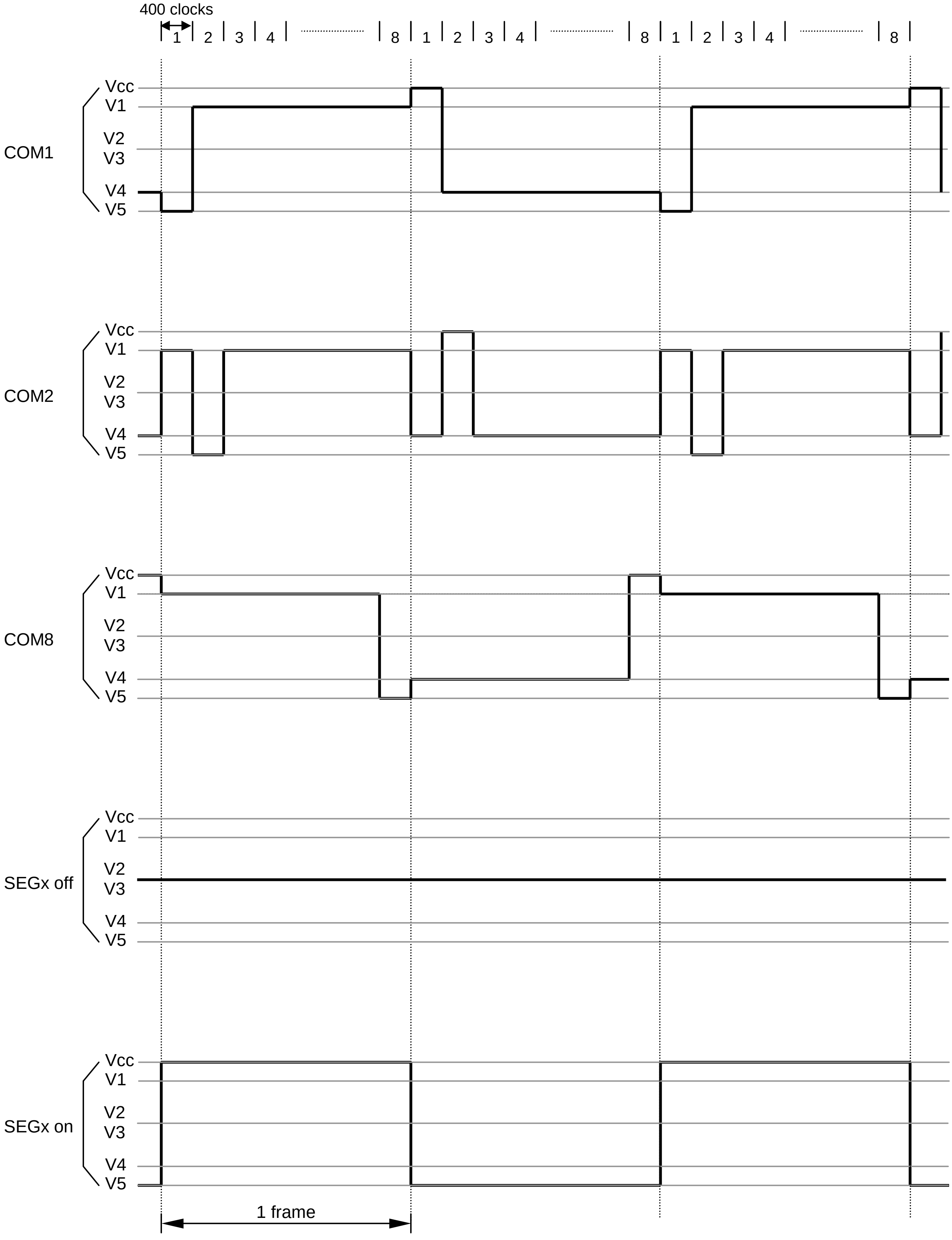
- **Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/16 duty; 1/5 bias,1 frame = 3.7us x 200 x 16 = 11840us=11.8ms(84.7Hz)**



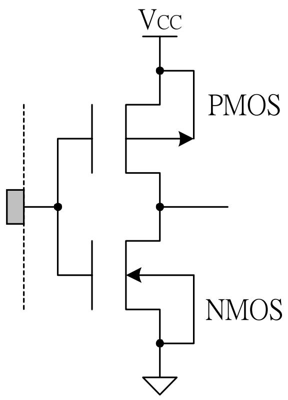
- **Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/11 duty; 1/4 bias,1 frame = 3.7us x 400 x 11 = 16280us=16.3ms (61.3Hz)**



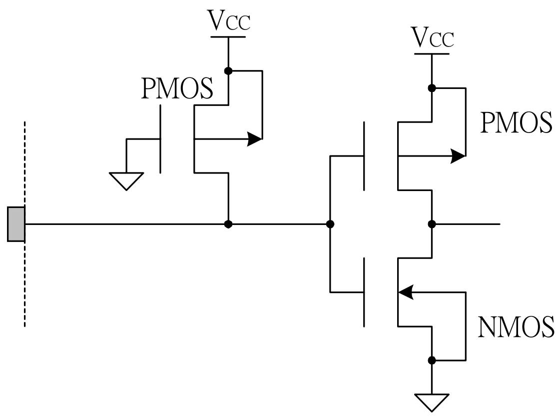
- **Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/8 duty; 1/4 bias,1 frame = 3.7us x 400 x 8 = 11840us=11.8ms (84.7Hz)**



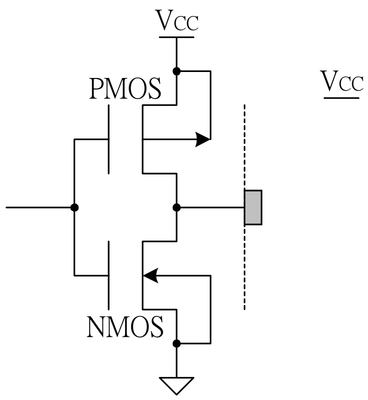
■ I/O Pad Configuration



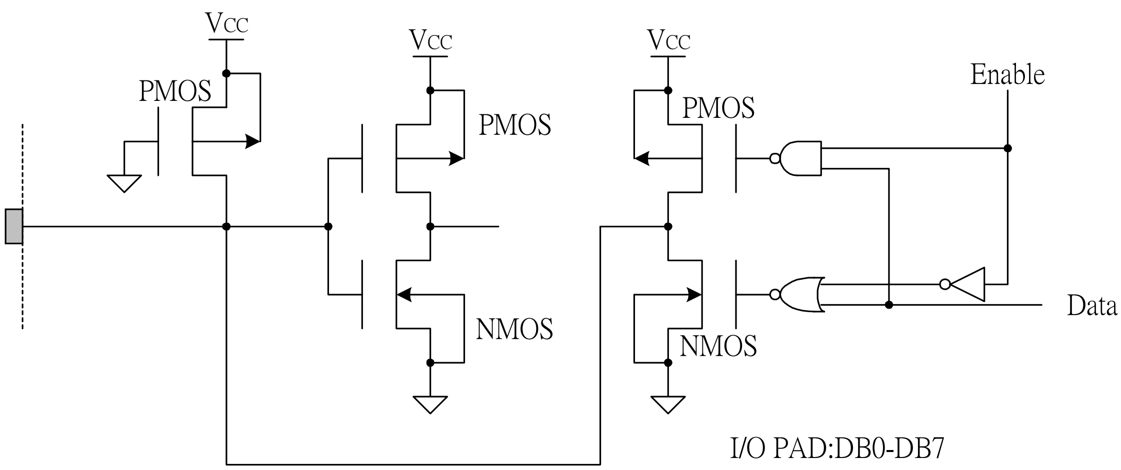
Input PAD:E(No Pull up)



Input PAD:RS,R/W(With Pull up)



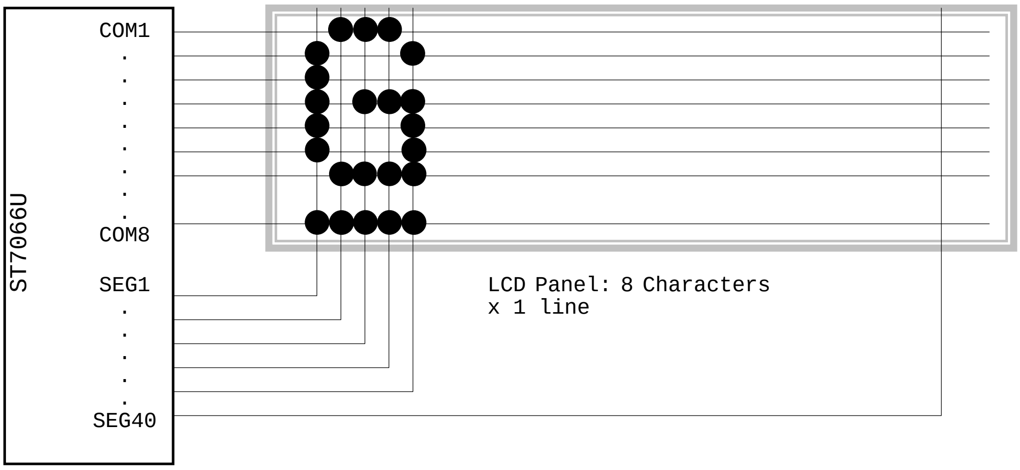
Output PAD:CL1,CL2,M,D



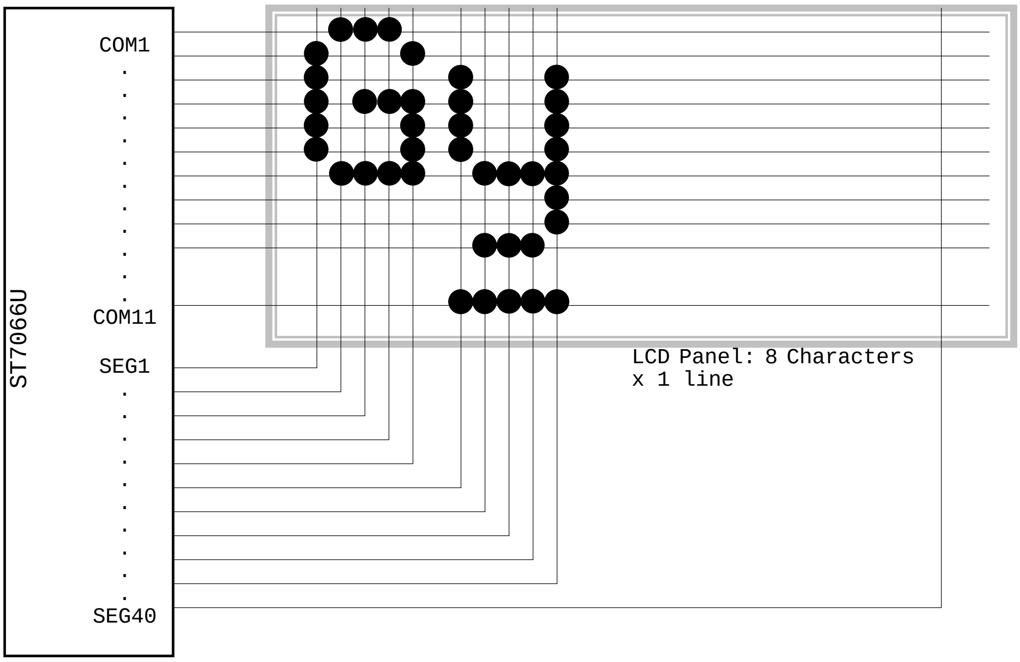
I/O PAD:DB0-DB7

■ LCD and ST7066U Connection

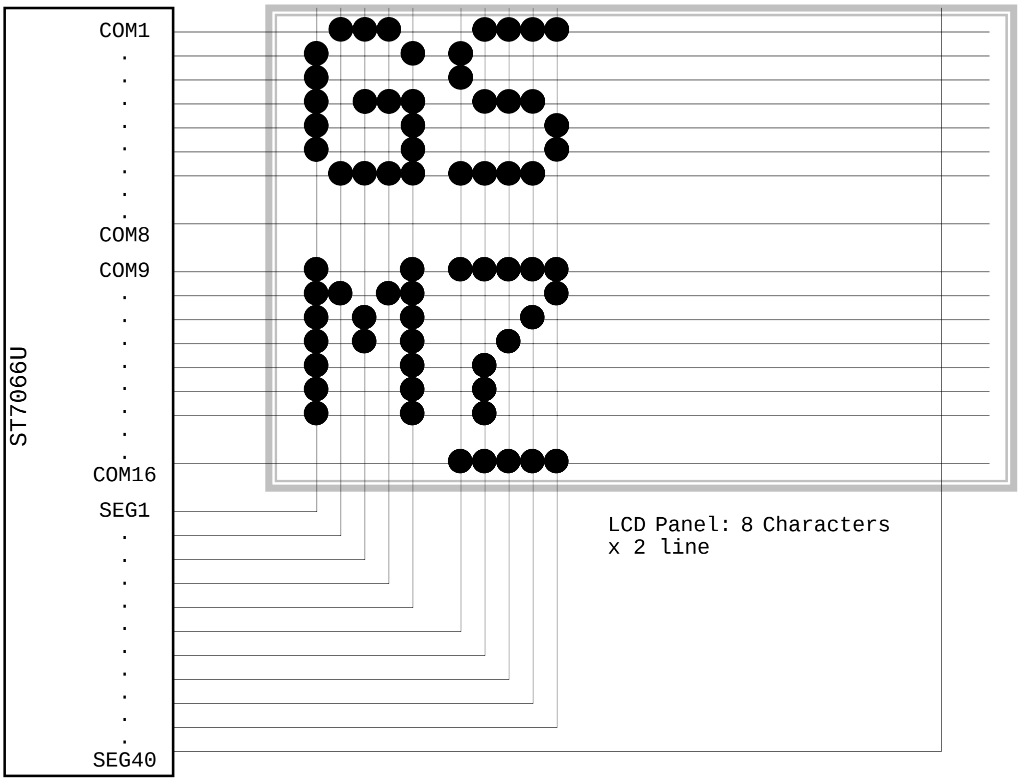
1. 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



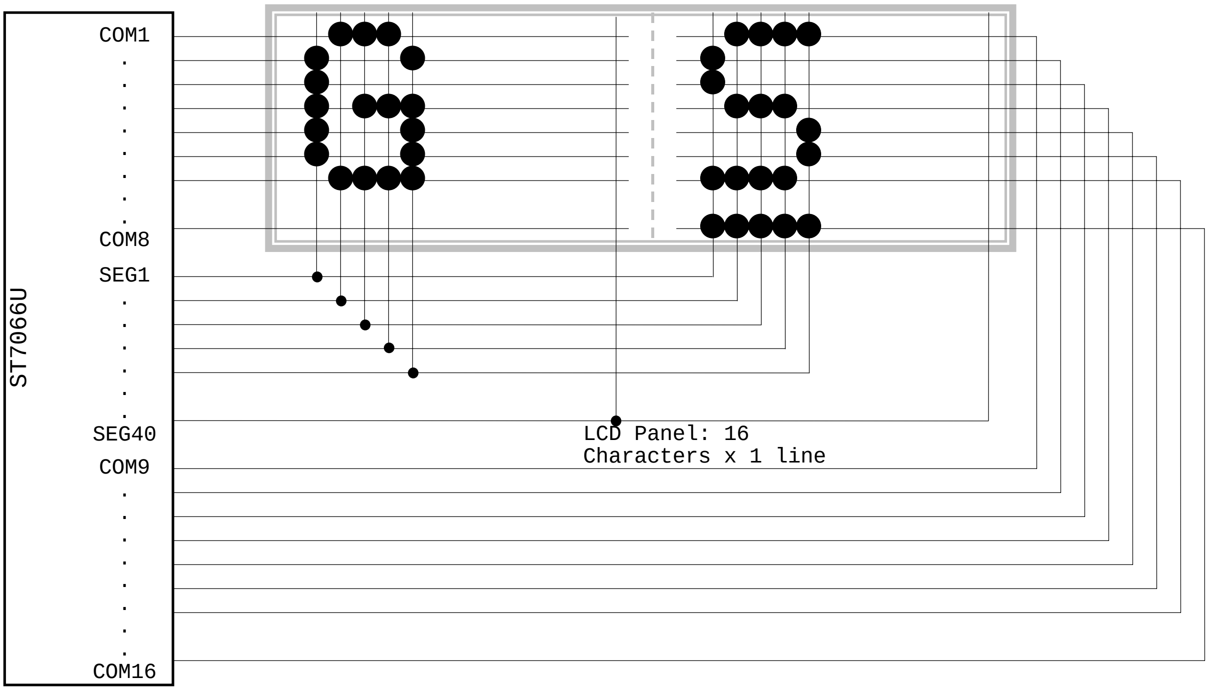
2. 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



3. 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



4. 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



■ Application Circuit

